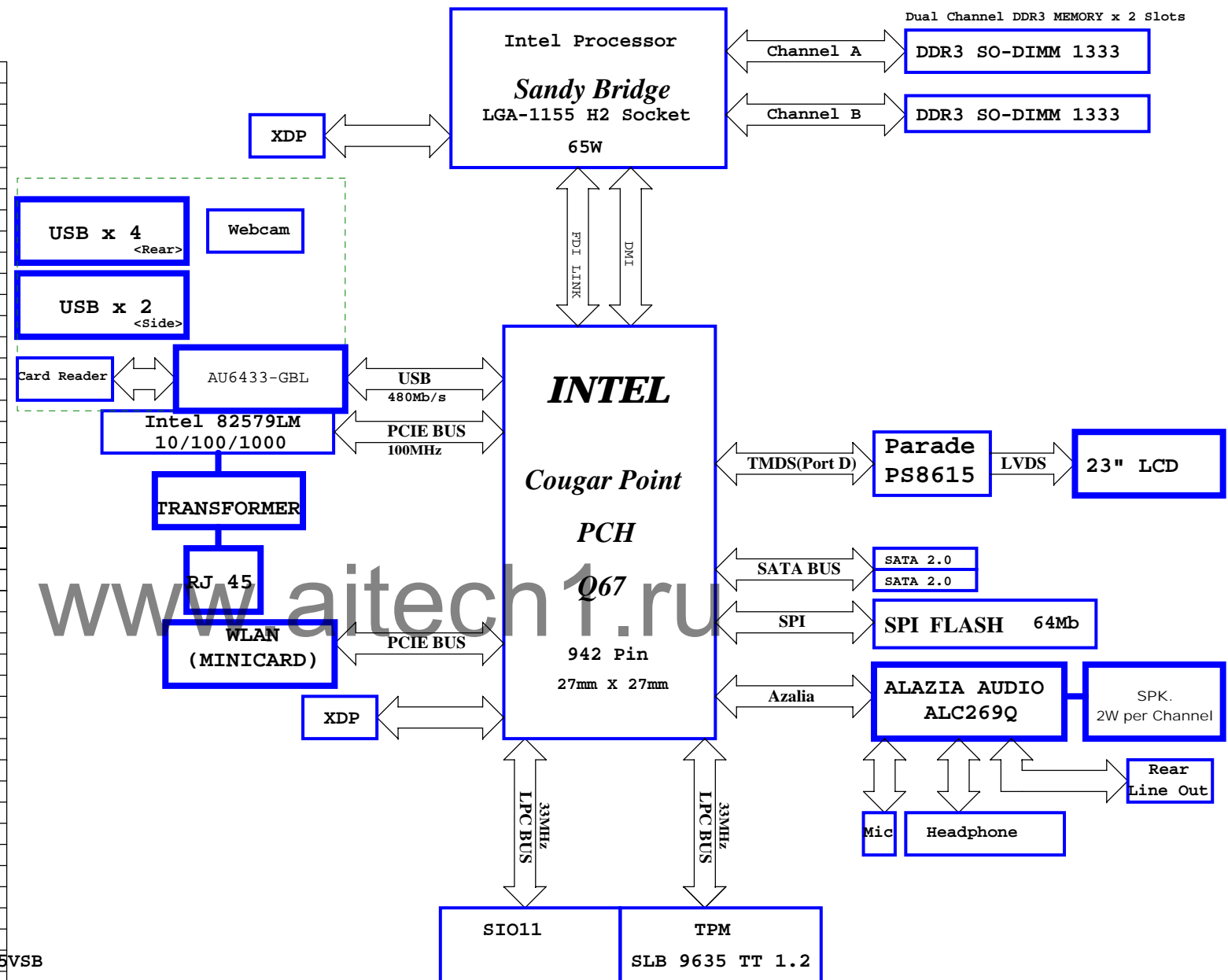


Revision: 1.00

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02	CHANGE HISTORY - 1
03	CHANGE HISTORY - 2
04	CHANGE HISTORY - 3
05	CLCOK DISTRIBUTION
06	SIGNAL&RESET MAP
07	POWER FLOW
08	POWER DISTRIBUTION
09	POWER SEQUENCE
10~15	Sandy Bridge LGA-1155
16	PLTRST_CPU#
17	DDR3 CHANNEL A
18	DDR3 CHANNEL B
19	DDR3 TERMINATION A&B
20	XXXXX
21~29	Cougar Point Q67
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31	PCH_DPWROK & SUS_ACK#
32	DEBUG VGA PORT
33	PANEL CONTROL
34	eDP TO LVDS
35	LVDS TO PANEL
36	WLAN
37	LEWISVILLE 82579LM
38	RJ45
39	FRONT PANEL
40	SCREW HOLE
41	WEBCAM & MIC
42	CARD READER
43	CODEC ALC269Q
44	COM HEADER
45	AUDIO JACK
46	TPM
47	SIDE USB
48	REAR USB
49	SATA CONN
50	SYSTEM FAN
51	SM BUS & SPI ROM
52	19V IN
53	+3VA,+5VA,+393V_MINI
54	+1P5V_DUAL,+1P5V
55	+VTT_DDR&+1P5V_DUAL_EN +3P3VSB,+
56	+19V,+5V,+3P3V
57	CURRENT METER & DEBUG LED
58	+5V_DUAL,+3P3V_DUAL
59	+12V,+1P8V_SFR
60	+1P05V_PCH
61	+3P3V_LAN +3P3V_ME,+1P5VSB,+1P05V
62	+1P05V_CPUIO,+0P925V_SA
63	+1P05V_CPUIO CAP
64~66	VCORE CONTROLLER
67	VCORE CAP

68	+V_AXG DRIVER
69	VCORE CAP
70	RTC/CMOS/SPKR
ME 71	BIOS and LPC header
72	CPU XDP DEBUG CONNECTOR
73	PCH XDP DEBUG CONNECTOR
74	SIO11-1
75	SIO11-2



PEGATRON DT-MB RESTRICTED SECRET			
PEGATRON		Title : BLOCK DIAGRAM	
Pegatron Corp.		Engineer: Scott Chen	
Size A3	Project Name IPISB-SB	Rev 1.00	
Date: Thursday, April 14, 2011		Sheet 1 of 73	

Schematics Change History

Observation Id: 720315 - VTT_DDR enable level too low
Change PR119 to 1Kohm,delete PQ44,PR164,PC248,PR379,add PC249/PQ78(NI)/PR419(NI).

Observation Id: 715089 - remove the EDID_WP# feature and releated circuit.
Delete R37438, R37439; install R85
R27, R28, R37401, R37402 change to RN4407 save layout space

Observation Id: 715087 - remove the FAB_ID[0:2] releated circuit and feature
Remove SR88, SR85, SR57; install SR64

Observation Id: 718216 - to meet Kona enterprise requirement (Connector Contact Plating)
Change DIMMA P/N to 12X2BBB2E011

Observation Id: 720317 - WLAN_DISABLE# pull-up is required
Delete Net:WLAN_DIS_SUS# (GPIO8) add SR112 for BRD_ID2
Delete Net:WLAN_DIS#,R37420;Add SR116 for GPIO33

Observation Id: 715248 - Need HP to define which GPIO of SIO11 will be for Brightness up/down and ODD
eject buttons.
Bright_up# change from PCH (GPIO31) to SIO11 (pin92) delete R37412
Bright_down# change from PCH(GPIO34) to SIO(pin95);delete R37411(internal debunce)
Install R7170, DELETE R37413

Observation Id: 720320 - Audio BEEP support
AUDIO_DISABLE change from PCH(GPIO32) to using SIO11 control (pin69) add SR115
Uninstall R7247,PR418; Install PQ77,R7221,PQ76,PQ74,R7234
Uninstall R37562,R37561; Install PQ79,PR90,PR91,PQ80,PR88,PR89,PQ81,PR116
delete D3601; C3623 change to 2.2uF;
delete Q56,R3620,ER103,R3619;R1219 change to reserved 0.1uF cap.Add Q9346,R37563

Observation Id: 720321 - Support BEEP from codec in S5 state
Audio codec pin39 pin46 change from core power to
standby power(+5VSB);

Observation Id: 716637 - Kona EVT2 system boards do not have a silkscreen for the four rear USB ports.
USB port 8 change to port12 and rename to USBN12,USBP12
Delete R7177,R7178(double PU)

Observation Id: 720464 - HD LED didn't meet PCA spec.
Delete ODD_LED#,R37448,D8823,TD1
R82 change to Pull-high standby power, and change to 75ohm

Observation Id: 720468 - DDR reset measurement fail
Add R37564,SQ9,R37565,R37566,R37567,SQ10,SQ11,R37569,R37568
Reserved SR284,SR285; delete SR283
R37565 change to pull-high +3vsb

Observation Id: 720322 - Clock should follow PCA spec
Change CK_33M_TPM to PCH ball AN14
Change CK_33M_PCIFB to PCH ball AT12
Change CK_33M_DEBUG to PCH ball AT14
Change CK_100M_PCHXDP to Port 7
Change CLK_PCIE_WLAN to port 6

Observation Id: 720324 - SM-Link didn't connect to SIO11
Add smbus link from PCH to SIO
Reserved SR117
Install SR85, uninstall SR64
Reserved SR48 add SR96

Observation Id: 718229 - to meet the enterprise requirement (Common Reference Designators)
Observation Id: 717253 - Kona EVT2 system boards FDO jumper is labeled as IE80.
Observation Id: 717255 - Kona EVT2 system boards do not have silkscreen labels for
Bootblock and Bootblock Recovery.
Add mini jumper E15:12 E14:12
Delete E69 E69:46 E69:35
Delete NET:Boot_BLK_WRITE_EN, R8826, R8824
P1 change to P5 Layout PB
P52 chnge to P54 Layout COMA
SU1 change to U4
U9382 Change to U5
LU1 Change to U10
AU3 Change to U13
IU1 Chnge to U19
U86 Change to U29
U8 Change to U31
U1 change to U40
HU1 change to XU1
Y3 (1.00) change to Y10 (1.01)
Y10 (1.00) change to Y3 (1.01)
LED2>CR1 Layout should use AUX
IE80>E1 Layout should use FDO BR8 move to pin 2 and change connector to 2 pin ,
remove R37445,
delete mini jumper IE80:23
E19>E14 Layout should use BB change to 2pin connector 12X602012B00 SR21
change to 8.2K
E18>E15 Layout should use BBR
JE16 >E16 Layout should use ROM RCVR mini jumper change to E16:12
J90>E17 Layout should use LPC
CON3813>J9 Layout should use RJ45
P69>J69 Layout should use VGA
J11>J70 ; J12 >J71 ; CON3807>J90 ; CON3806>J91 ;CON3804>J81 ; CON3805>J82
Layout should use USB
J87>J72 Layout should use MIC
J89>J74 Layout should use OUT
J76>J75 Layout should use HDPH
J9>J103 Layout should use PWR
J61>J105 Layout should use X1PCIEXP11
PWR_CON1>P1 Layout should use PWR
CON3814>P6 AND CON3815 Layout should use SPKR
P30>P8 Layout should use CPUFAN
P29>P9 Layout should use CHFAN
P116>P160 Layout should use SATA PWR0
P114>P161 Layout should use SATA PWR1
DIMMA0>XMM1 Layout should use DIMM1
DIMMB0>XMM3 Layout should use DIMM3
XBT2>XBT1 Layout should use BATTERY
Install R4707 720317
SW51 change to 2pin connector 12X400120B20 change ref to E49 Layout should use PSWD
SW50 change to button type

Schematics Change History

Observation Id: 720471 - Board ID should follow PCA spec
Delete SR108 change BRD_REV1 to use stand by power uninstall SR87 install SR91

Observation Id: 720326 - Debug LED and Serial port didn't meet PCA spec
Change serial port solution
 delete Q8,R37407,R37408,Q15,R16
R8831,Q9348,CR7,R4819,R8830,CR6,Q9347,R4818,CR8,R8832,R4822,
 Q9349,R8833,CR10,Q9350,R4823 net SLP_A#,SLP_S5#,SLP_SUS#,SLP_LAN#
Add U7204 for Serial port function

Observation Id: 720475 - GPIO should follow PCA spec
Reserved SR113 for USB detec control
Add SR114
Add COMM_B_DET# CONNECT TO GPIO69
Install SR50,

Observation Id: 720452 - Power noise fail with VccCikDMI and +5VSB
SR163 change to 0 ohm, follow CRB
change PR339 to 97.6 K and PR321 to 24 K can fix +5V noise issue.
Uninstall SR261 install SR259

Observation Id: 720456 - Power Status LED didn't meet PCA spec
Change Power LED design for PCA spec.

Observation Id: 721236 - O2R122 should chane to un-install

Observation Id: 714716 - please impenentation the DC INRUSH CIRCUIT
Add at page 55

Observation Id: 718222 - to meet enterprise PCa requirement (Smart ID)
Add at page 76

Observation Id: 719021 - Kona EVT2 system can't detect mini PCIe ETD device.
Observation Id: 719694 - Kona EVT2 systems do not have R4706 installed for the mini-PcIe slot 1.5V
Add at page 36

Reduce power consumption in DSW mode
1).R364 change to 2K
2).PR22 change to 2K
3).Remove SR196, SR199, SR188, SR189, SR190

Delete PR327,PR330 ,U9378 ,C9352 ,SR133 ,SR134 ,U9379,R37418, R37450, PC329, PQ506,R37449, PC328
delete ECA5

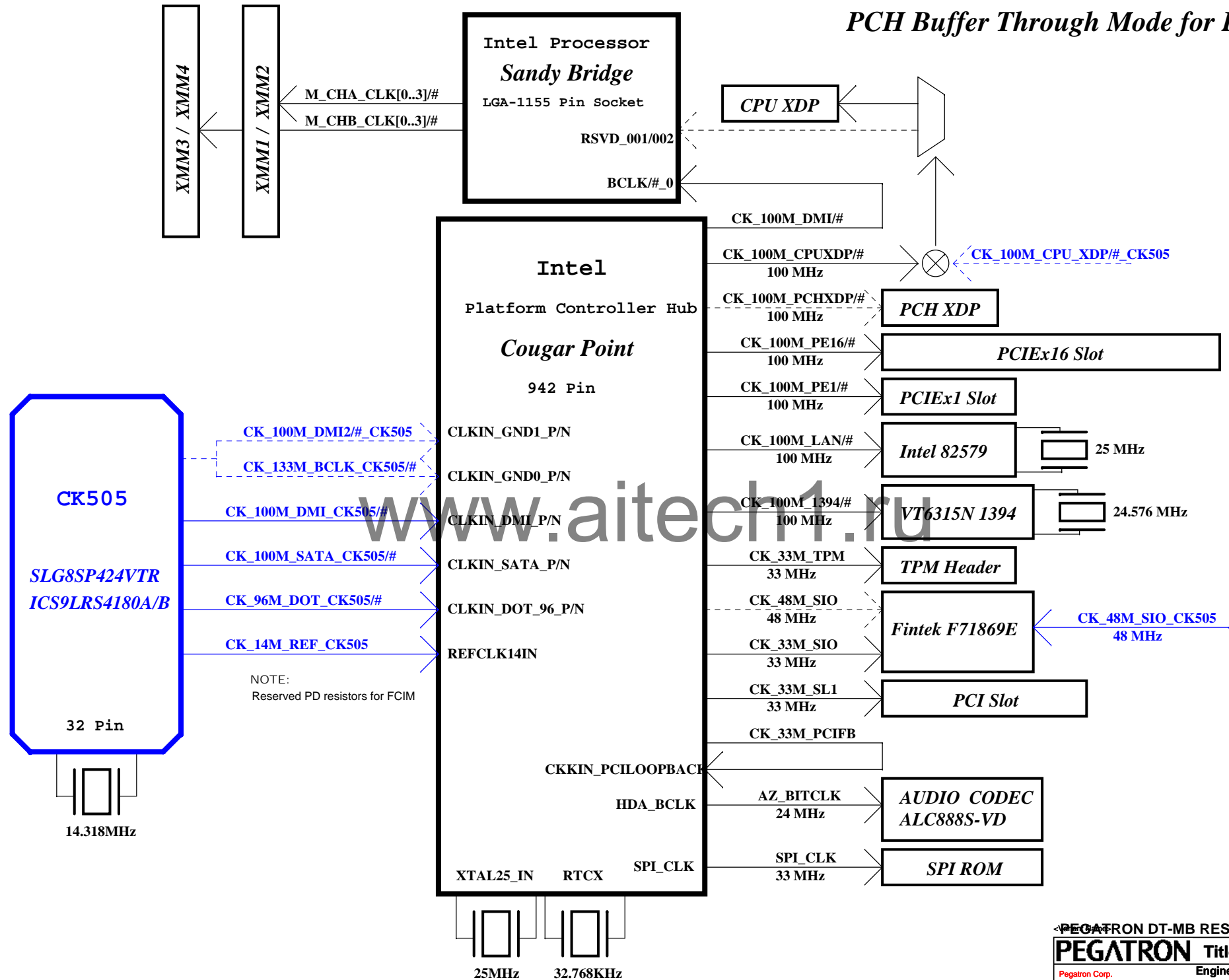
Power modify
1).Add PR196,PC178

Thermal issue
3).delete PPQ56 and relate circuit, add PU3/PC20/PC23.
 delete PR381/PR384/PR406/PR410,PR382/PR386/PR407/PR411 change to NI.
 add PC25(NI)/PC32(NI).
 PQ64 change to 07X50S211059.
 PQ24/PQ28/PQ67/PQ58 to NI.PQ25/PQ29/PQ69/PQ60 to Critical

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PEGATRON		Title : CHANGE HISTORY-3	
<small>Pegatron Corp.</small>		Engineer: Scott Chen	
Size	Project Name		Rev
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PCH Buffer Through Mode for Pre-Silicon



<Verbatim Name> PEGATRON DT-MB RESTRICTED SECRET

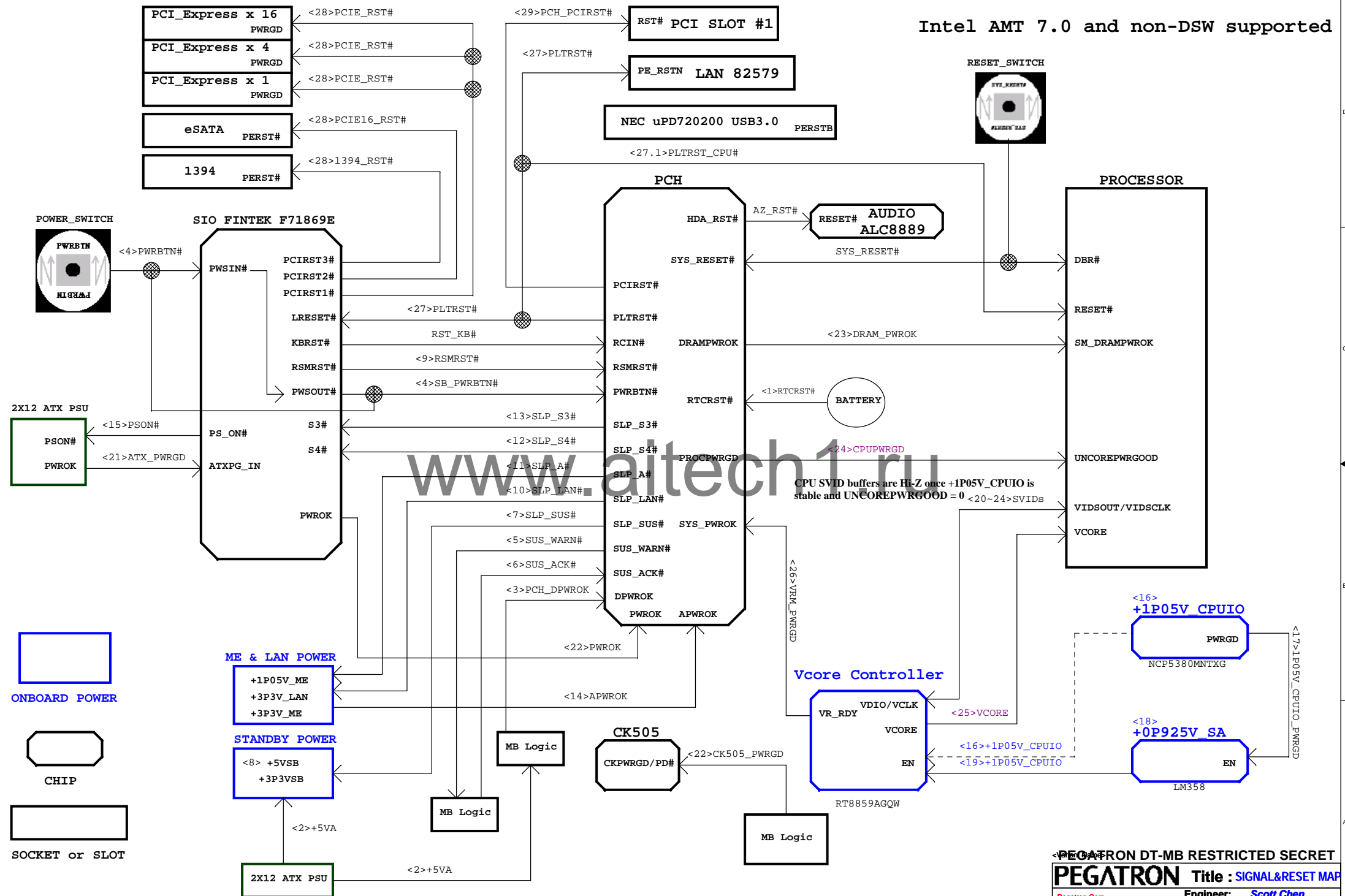
PEGATRON Title : CLCOK DISTRIBUTION

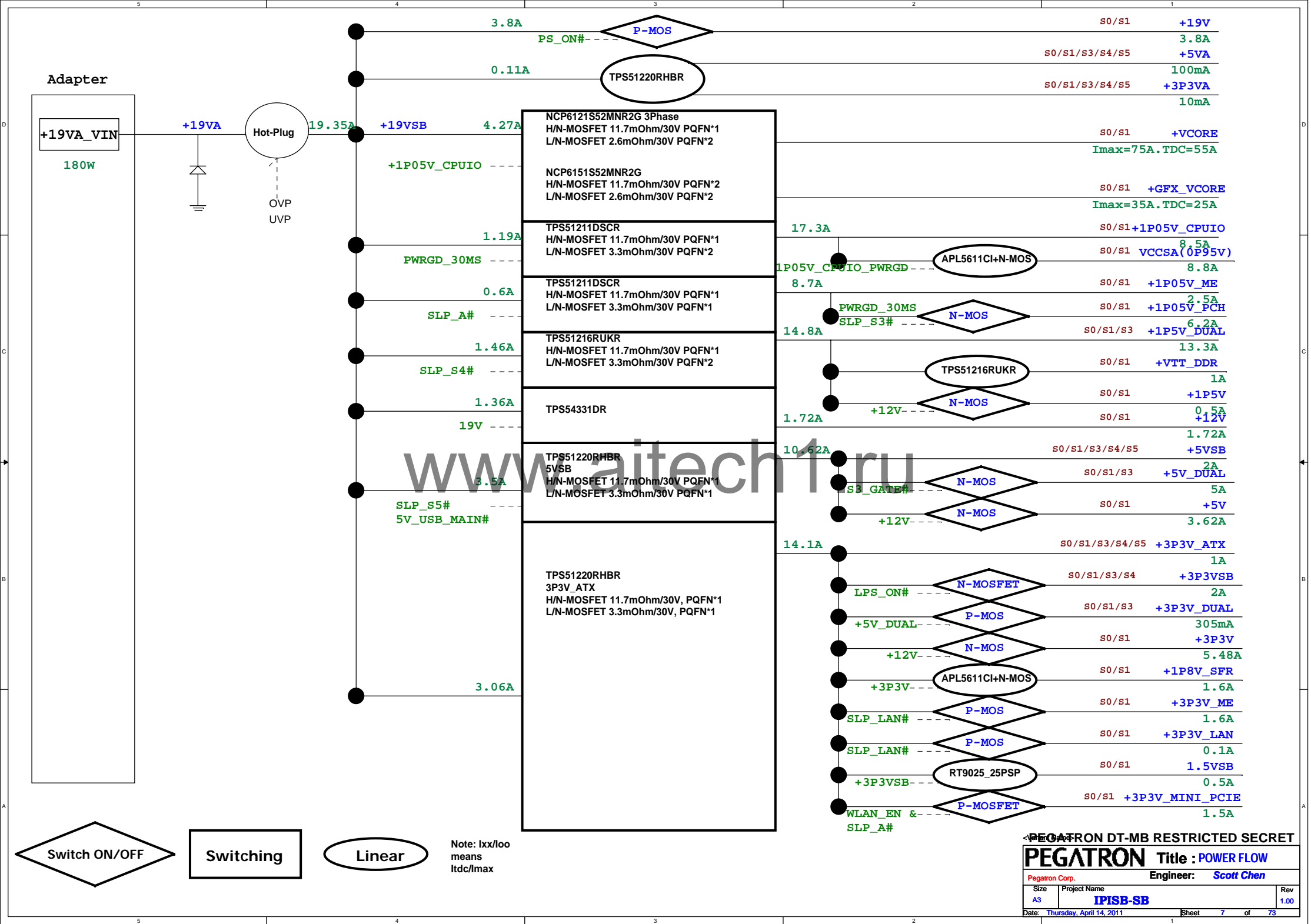
Pegatron Corp. **Engineer:** **Scott Chen**

Size	Project Name	Rev
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Intel AMT 7.0 and non-DSW supported



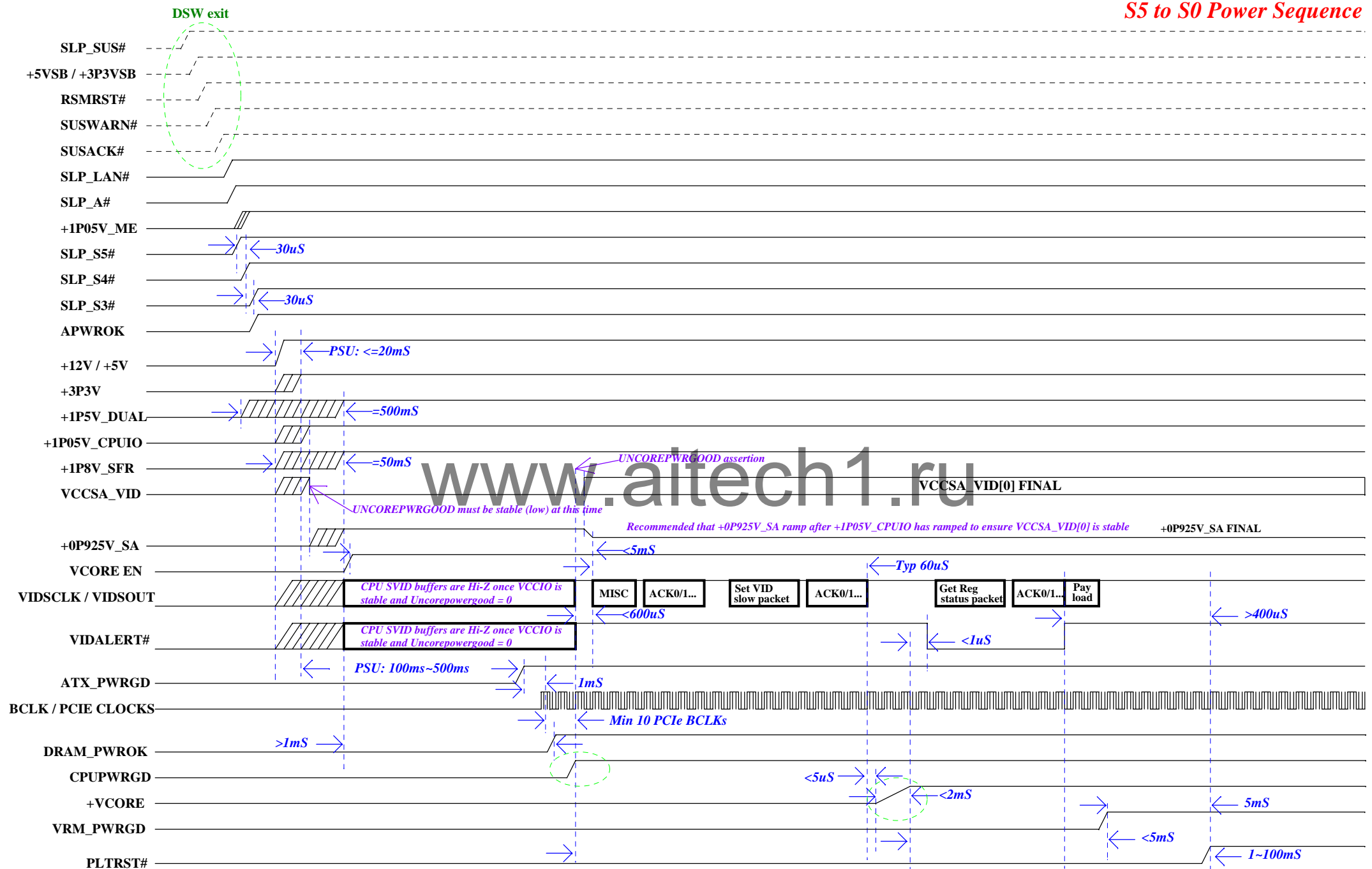


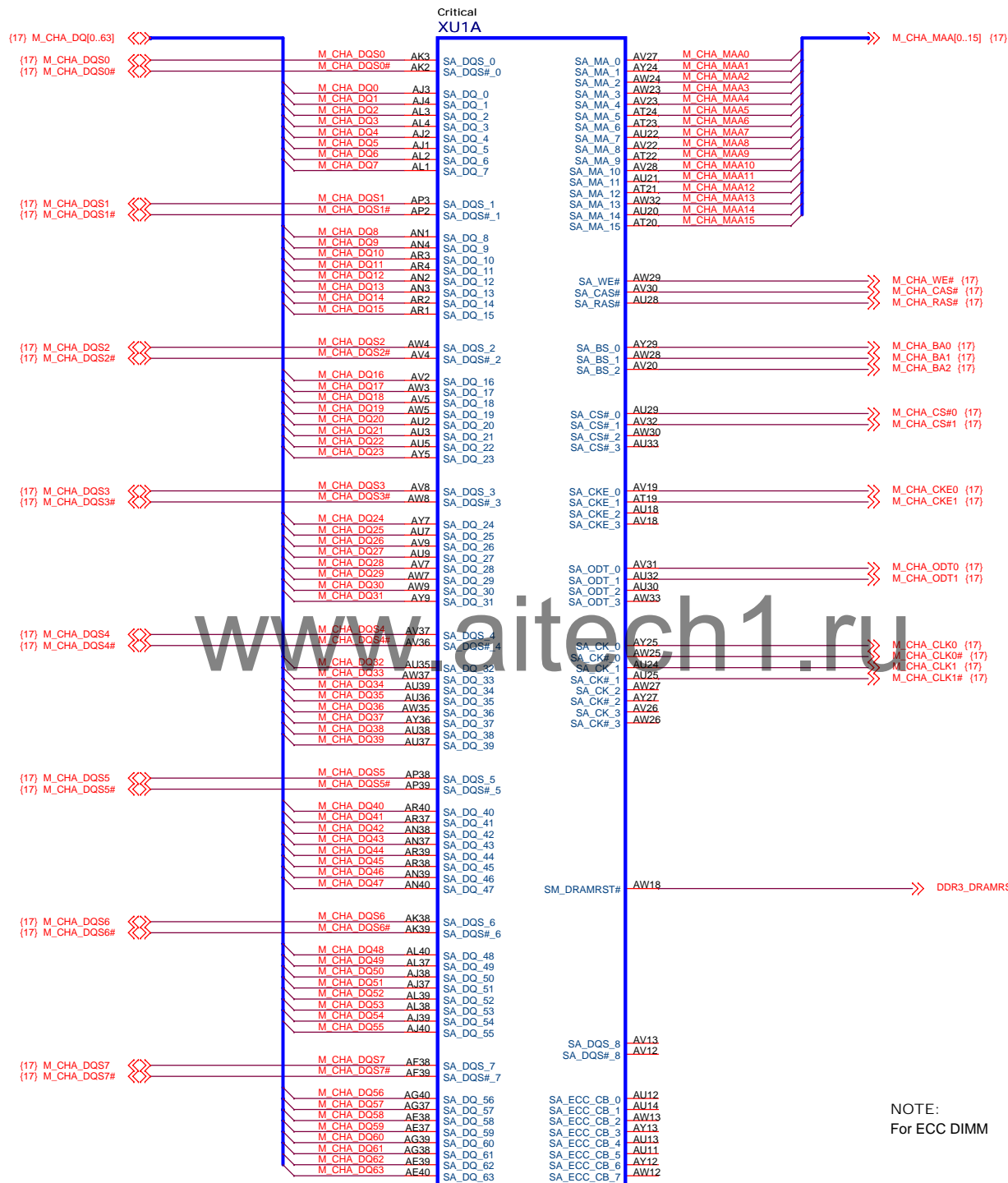
	CPU Sandy Bridge
+VCORE	-> 95A (TDC) - 95W
+1P05V_CPUIO	-> 17A (Imax) - W
+0P925V_SA	-> 8.8A (Imax) - W
+V_AXG	-> 25A (TDC) - W
	CLOCK GEN
+3P3V	-> 125mA - W
	PCH
+1P05V_PCH	-> 5.831A - W
+1P05V_CPUIO	-> 0.043A - W
+1P8V_SFR	-> 0.16A - W
+3P3V	-> 0.267A - W
+3P3VSB	-> 0.107A - W
+1P05V_ME	-> 1.01A - W
+3P3V_ME	-> 0.02A - W
+3P3VA	-> 0.002A - W
+BATT	RTC (G3) -> 6uA - 0.0198mW
	DDR2 DIMM (4) & Termination
+1P5V_DUAL	VDD (S0, S1, S3) -> 7.5 A - 11.25W
+VTT_DDR (0.75V)	SM VTT (S0, S1) -> 1A - 0.75W

	PCI Express x 1
+12V	-> 5A - 60W
+3P3V	-> 3.0A - 9.9W
+3P3VSB	WAKE -> 0.375A - 1.24W No WAKE -> 20mA - 66mW
	PCI Express x 16
+12V	-> 5.5A - 66W
+3P3V	-> 3.0A - 9.9W
+3P3VSB	WAKE -> 0.375A - 1.24W No WAKE -> 20mA - 66mW
	PCI SLOTS
+12V	-> 0.5A - 6W
-12V	-> 0.1A - 1.2W
+5V	-> 5.0A - 25W
+3P3V	-> 7.8A - 25.08W
+3P3VSB	WAKE -> 0.375A - 1.24W No WAKE -> 20mA - 66mW
	INTEL 82579
+3P3V_LAN	-> mA - 720mW
	SIO Fintek F71869E
+3P3V	-> 35mA - mW
	ALC888S-VD Codec
+3P3V	-> mA - mW

	NEC uPD720200 USB3.0
+3P3V	-> 15mA - W
+1P05V_USB	-> mA - W
	USB 14 PORTS
+5V_DUAL_B/F	(S0, S1) -> 7A - 35W
	1394A VT6315N
+3P3V	-> mA - W
	HDMI
+5V	-> mA - mW -> mA - mW
	DVI
+5V	-> mA - mW -> mA - mW
	DP
+3P3V	-> mA - mW -> mA - mW
	FANS
+12V	-> 1.2A - 14.4W
	PS2 KB/MS
+5V_DUAL	(S0, S1) -> 0.345A - 1.73W (S3) -> 2mA - 10mW
	SPI
+3P3V_ME	-> 30mA - 99mW

S5 to S0 Power Sequence





DDR3_A

SOCKET_1155P

NOTE:
For ECC DIMM

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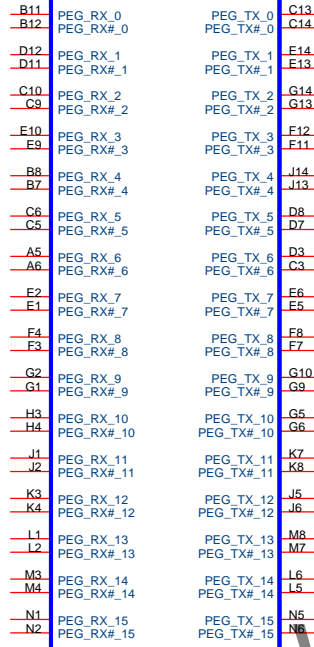
PEGATRON Title : DDR3_A 1-6

Pegatron Corp. Engineer: Scott Chen

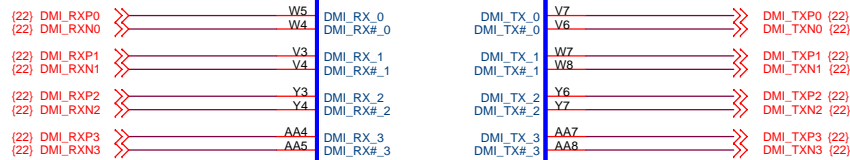
Size A3 Project Name IPISB-SB Rev 1.00

Date: Thursday, April 14, 2011 Sheet 10 of 73

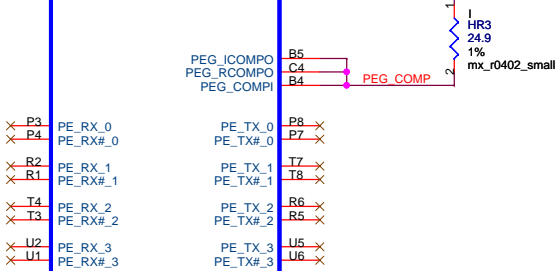
Critical
XU1C



PEG



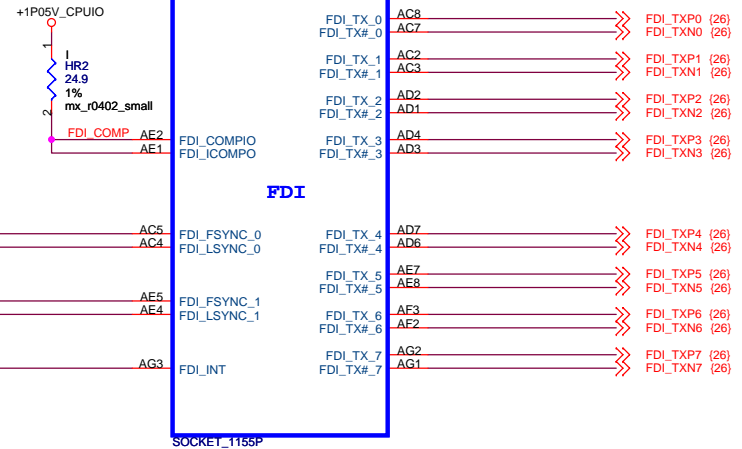
DMI



GEN

SOCKET_1155P

Critical
XU1D



FDI

SOCKET_1155P

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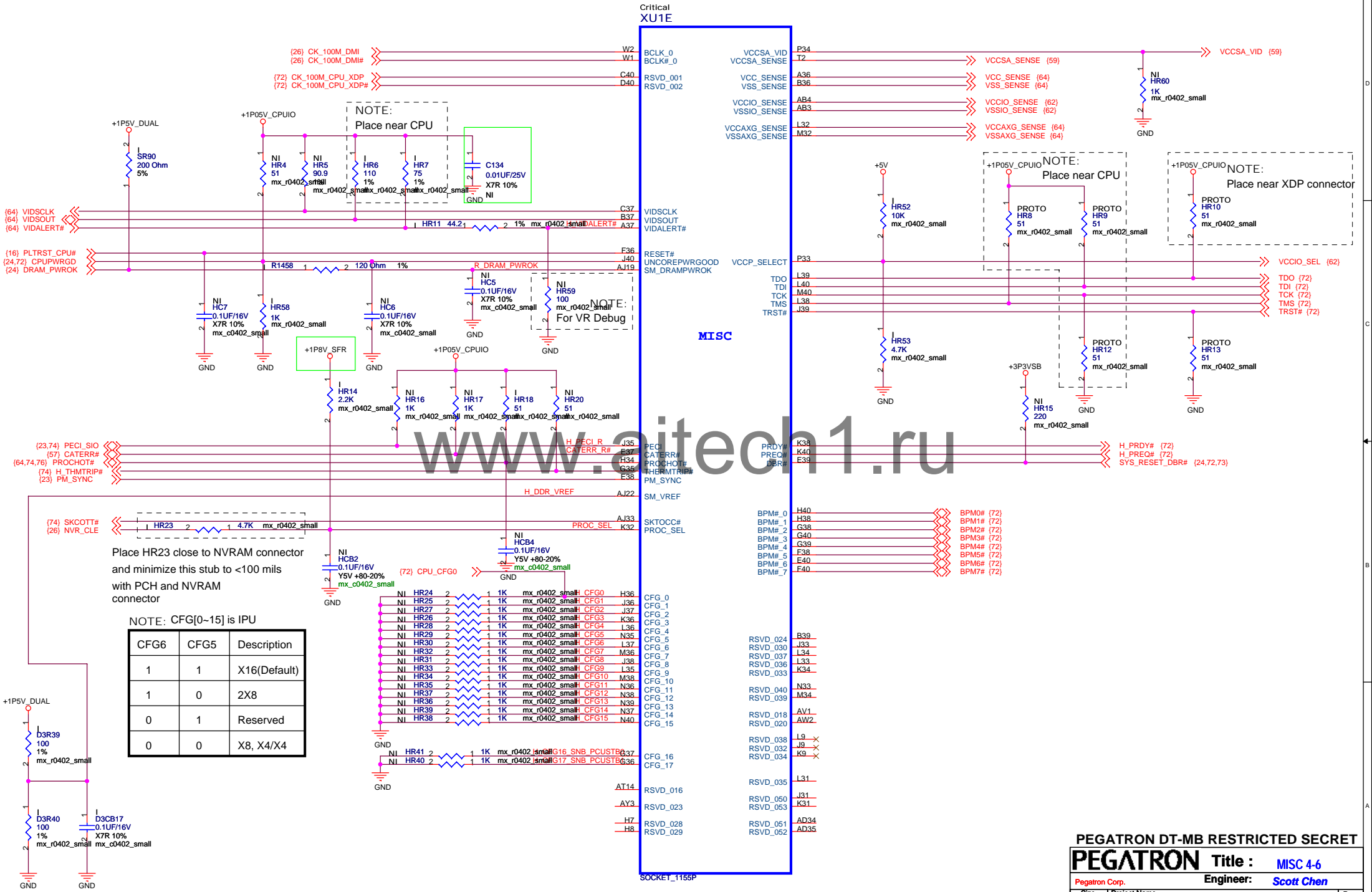
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PEGATRON Title : PCIE/DMI/FDI 3-6

Pegatron Corp. Engineer: Scott Chen

Size A3	Project Name IPISB-SB	Rev 1.00
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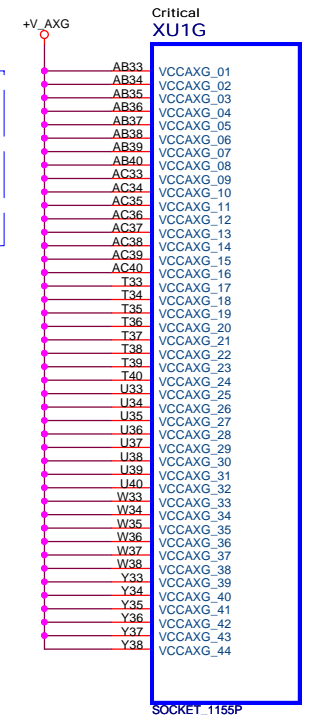
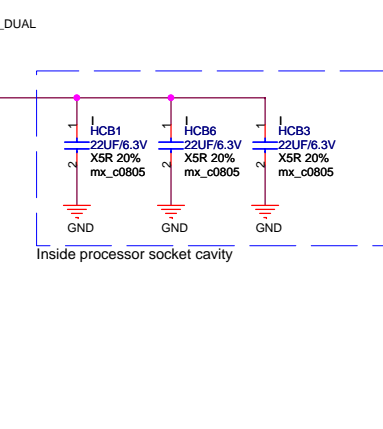
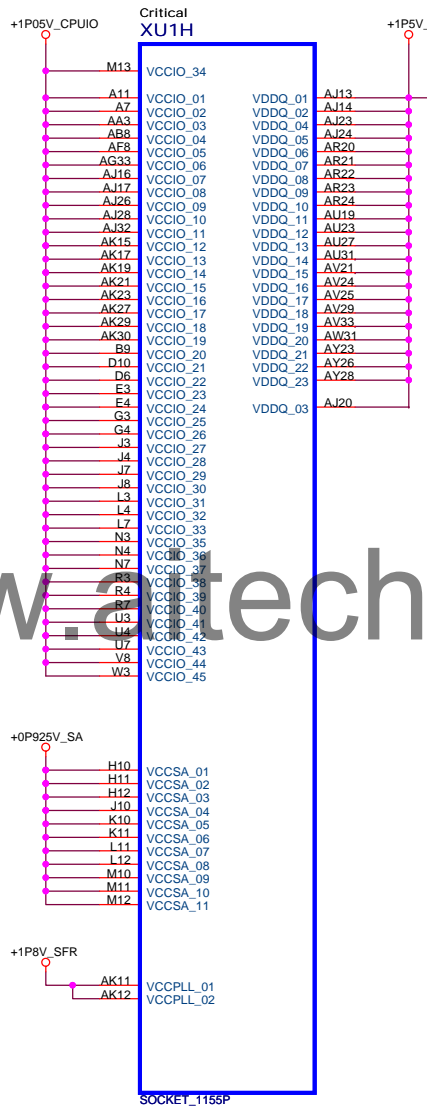
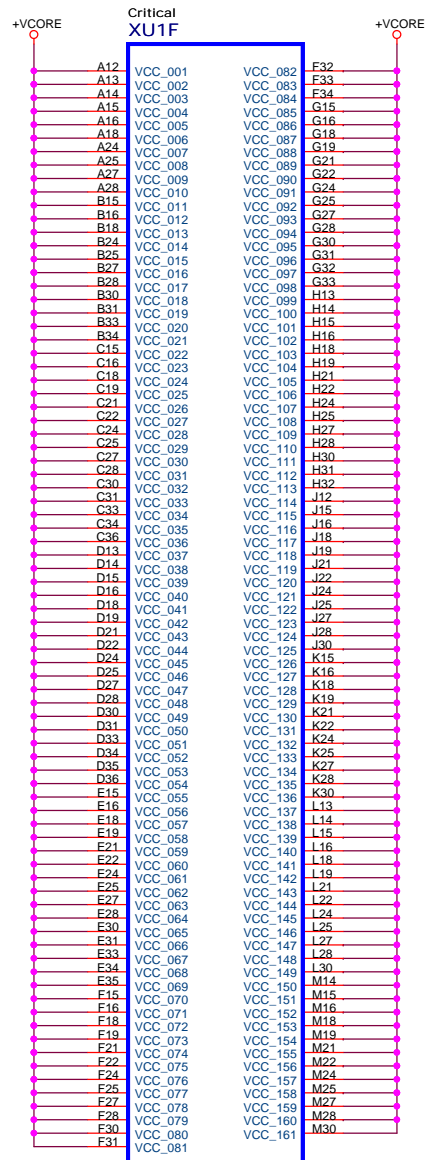
PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : **MISC 4-6**

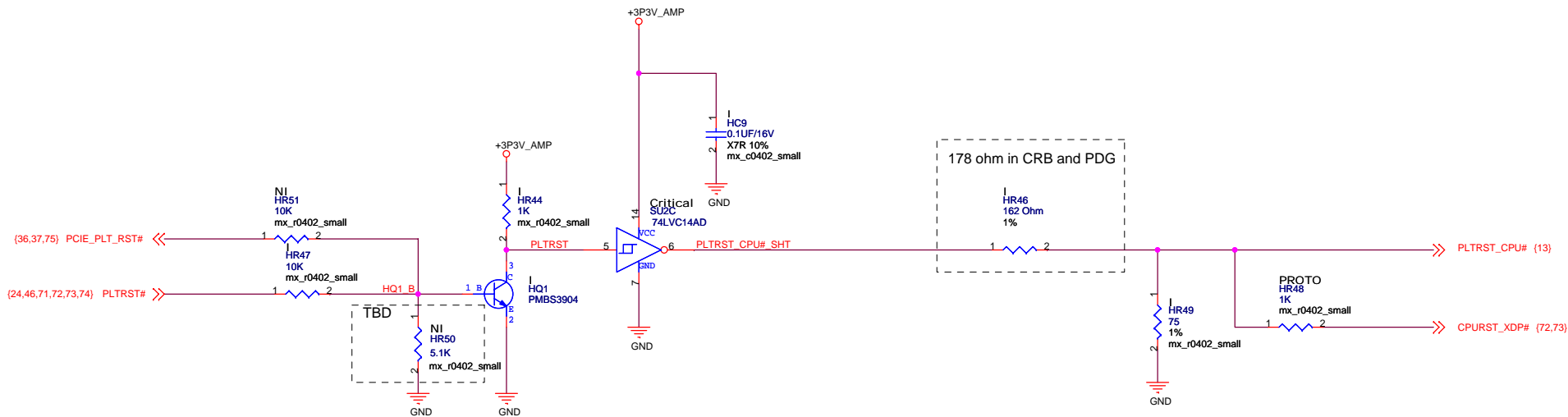
Pegatron Corp. Engineer: **Scott Chen**

Size **A3** Project Name **IPISB-SB** Rev **1.00**

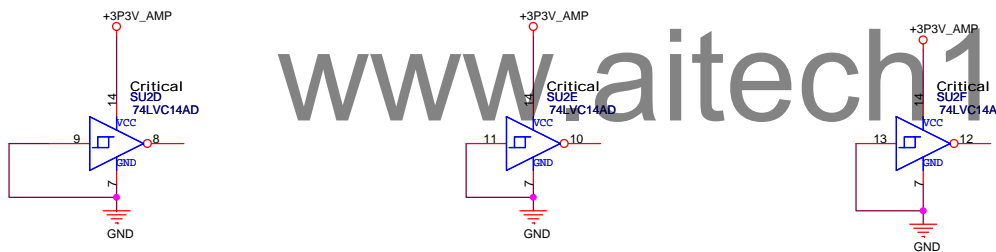
Date: **Thursday, April 14, 2011** Sheet **13** of **73**



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PLTRST_CPU#



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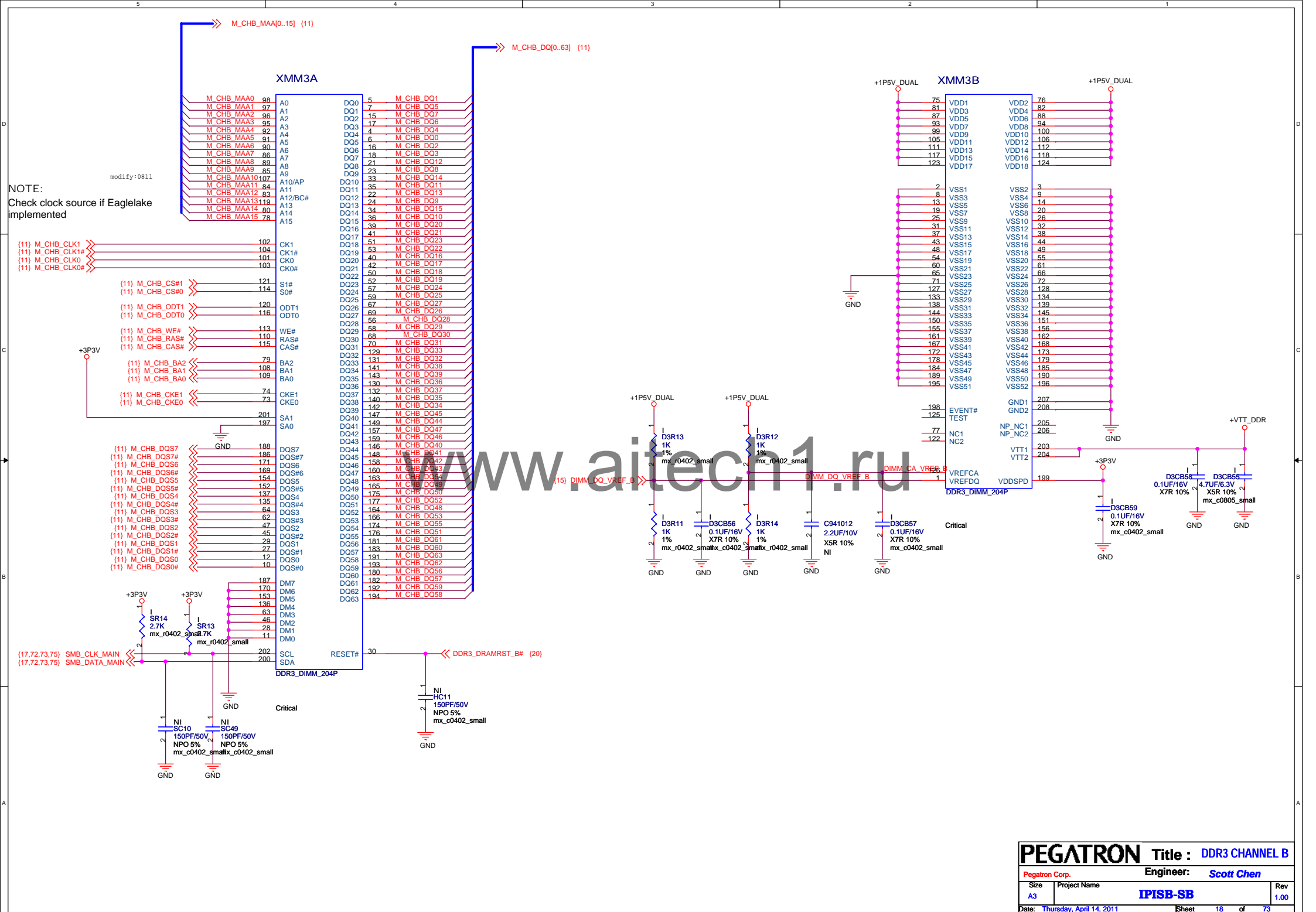
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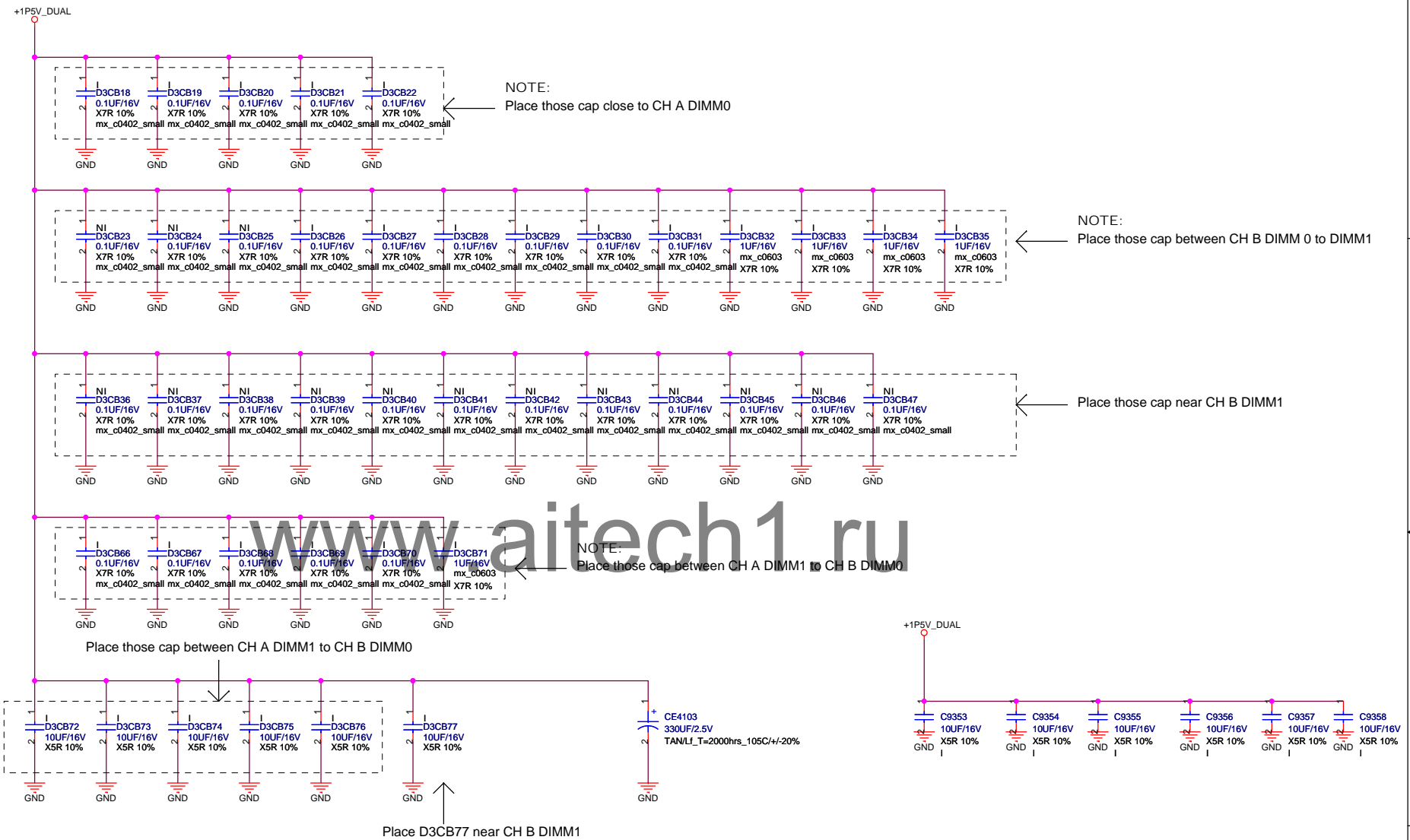
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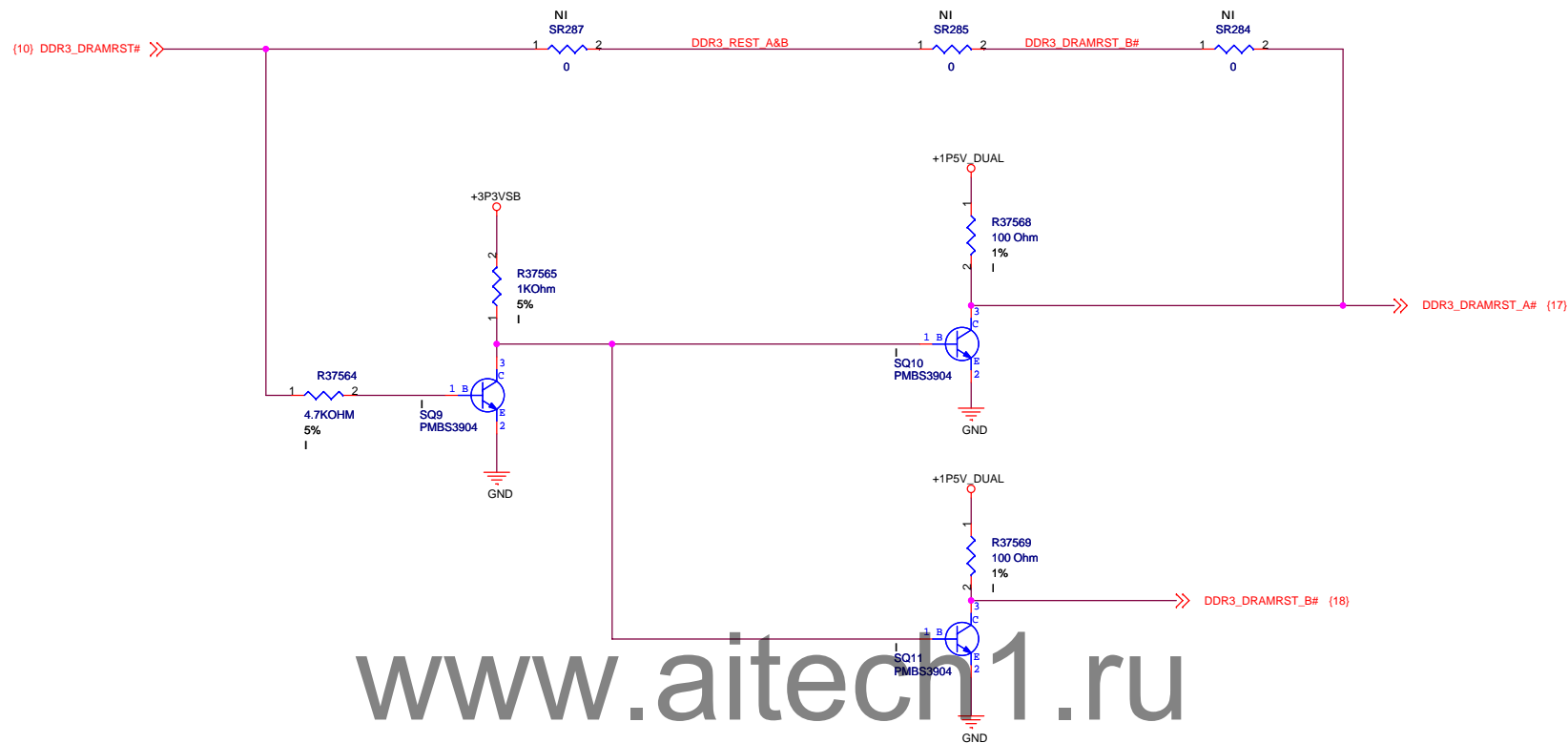
Pegatron Corp. Engineer: **Scott Chen**

Size A3	Project Name IPISB-SB	Rev 1.00
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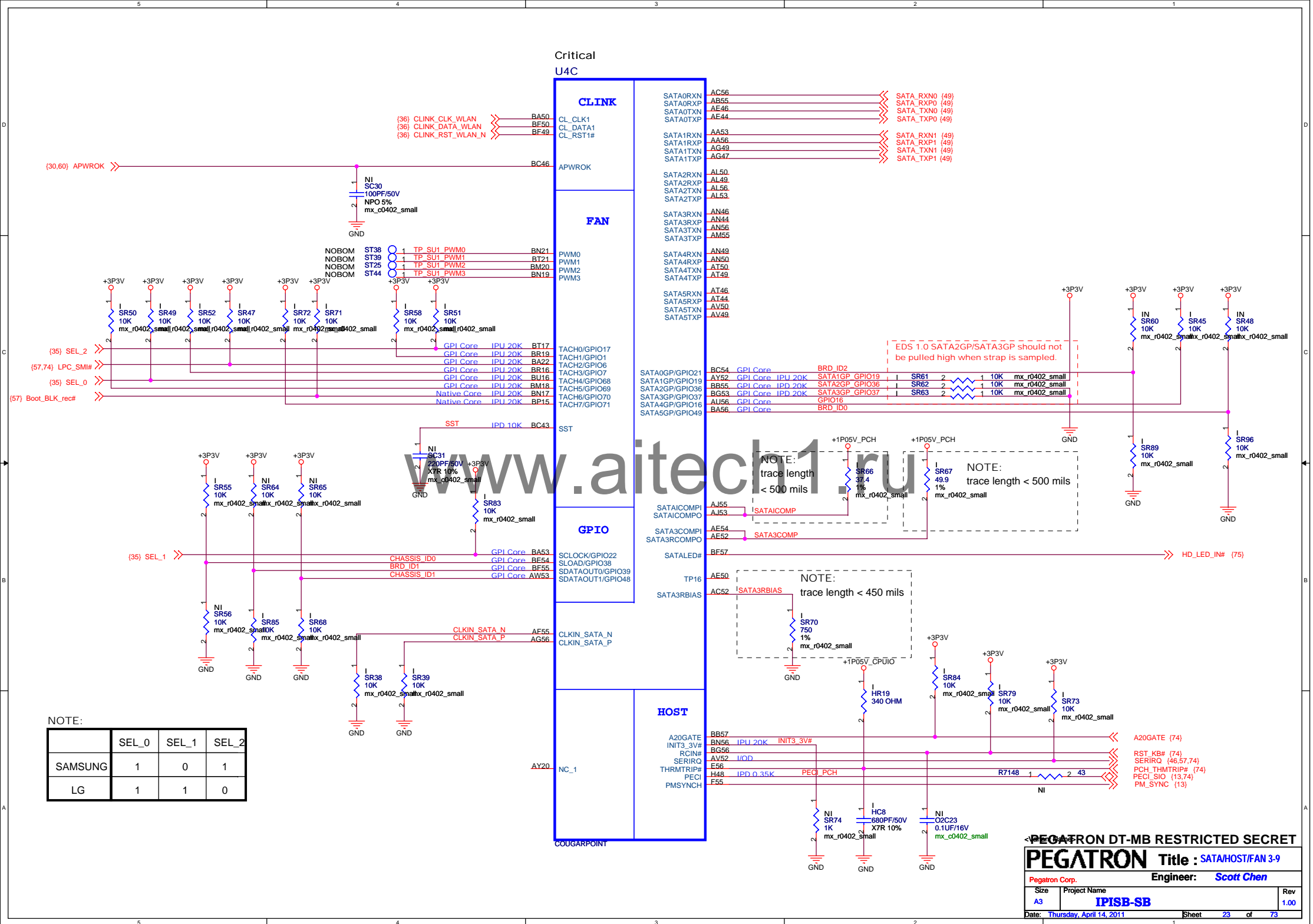
PEGATRON Title : RSMRST#

Pegatron Corp. Engineer: Scott Chen

Size	Project Name	Rev
A3	IPISB-SB	1.00

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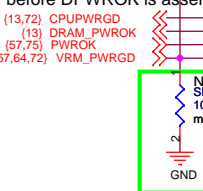
Date: Thursday, April 14, 2011 Sheet 21 of 73



NOTE: HDA_SYNC
On-die PLL VR voltage selector.
Hi: supplied by 1.5V.
Low: supplied by 1.8V.

NOTE: HDA_SDO
Disable ME in Manufacturing Mode
--> connect to GND.

NOTE:
For platform not supporting deep
sleep connect directly to RSMRST#.
The DSW rails must be stable for at least 10 ms
before DPWROK is asserted to PCH.



(16,46,71,72,73,74) PLTRST#
(13,72,73) SYS_RESET_DBR#
(73,74) RSMRST#
(31,73) PCH_DPWROK

(31) SLP_SUS#
(75) LPS_ON#

Critical U4D

LPC

LDRQ1#/GPIO23
FWH0/LAD0
FWH1/LAD1
FWH2/LAD2
FWH3/LAD3
LDRQ0#
FWH4/LFRAME#
BG17

AUDIO

HDA_SDO
HDA_SYNC
HDA_BCLK
HDA_RST#
HDA_SDIN0
HDA_SDIN1
HDA_SDIN2
HDA_SDIN3

JTAG_TMS
JTAG_TDO
JTAG_TDI
JTAG_TCK
TP12

PROC_PWRGD
DRAM_PWRGD
PWROK
SYS_PWROK

DSWVRMEN
INTVRMEN
PLTRST#
SYS_RESET#

RSMRST#
DPWROK
COUGARPOINT

BMBUSY#/GPIO0
CLKRUN#/GPIO32
HDA_DOCK_EN#/GPIO33
STP_PCI#/GPIO34
GPIO35
GPIO36
LAN_PHY_PWR_CTRL#/GPIO12
HDA_DOCK_RST#/GPIO13
GPIO15
GPIO24/MEM_LED
GPIO28
SLP_LAN#/GPIO29
GPIO27
GPIO31

PCIECLKRQ2#/GPIO20
PCIECLKRQ5#/GPIO44
PCIECLKRQ6#/GPIO45
PCIECLKRQ7#/GPIO46
GPIO57

BATLOW#/GPIO72
SUSWARN#/SUSPWRDNACK#/GPIO36
SUSACK#
SUSCLK#/GPIO62
SUS_STAT#/GPIO61

RI#
WAKE#
INTRUDER#
SPKR

PWRBTN#
SLP_S3#
SLP_S4#
SLP_S5#/GPIO63
SLP_A#
SLP_SUS#

SLP_S3# (54,57,60,74)
SLP_S4# (53,54,57,58,74)
SLP_S5# (53,57,74)
SLP_A# (30,57,60,61)
SLP_SUS# (31,57,75)

SLP_S3#
SLP_S4#
SLP_S5#
SLP_A#
SLP_SUS#

AW55 GPI Core
BC56 GPO Core
BC25 GPO Core
BL56 GPI Core
BJ57 GPO Core
BP51 GPO Sus IPU 20K
BK50 Native Sus
BA25 GPI Sus
BM55 GPO Sus IPD 20K
BJ55 GPO Sus IPU 20K
BH49 GPI Sus
BJ43 GPO DSW IPU 20K
BG43 GPI DSW IPD TBD

AV43 Native Core
BL54 Native Sus IPU TBD
AV44 Native Sus IPU 20K
BP55 Native Sus IPU 20K
BT53 GPI Sus

PCIECLKRQ5# GPIO44
PCIECLKRQ6# GPIO45
PCIECLKRQ7# GPIO46
NI SR141
NI SR256
NI SR180

NI SR183
NI SC47
NI SC45

NI SR75
NI SR76
NI SR77
NI SR78

NI SR132
NI SR133

NI SC25
NI SC29
NI SC33
NI SC39
NI SC41
NI SC47
NI SC45

STP_PCI# GPIO34
BRD_REV0
TP GPIO15
BRD_REV1

LAN_CLK_REQ# (37)
LAN_DISABLE# (37)
SLP_LAN# (57,61)

SUS_WARN# (31)
SUS_ACK# (31)
SUS_CLK# (46,75)

LPC_PME# (74)
WAKE# (36,75)

SPKR (43)
SB_PWRBTN# (74)

SLP_S3# (54,57,60,74)
SLP_S4# (53,54,57,58,74)
SLP_S5# (53,57,74)
SLP_A# (30,57,60,61)
SLP_SUS# (31,57,75)

SLP_S3#
SLP_S4#
SLP_S5#
SLP_A#
SLP_SUS#

SR116
SR100
SR115
SR105
R37442
SR103
SR109
SR110

SR107
SR124
SR159
SR123
SR132

SR183
SC47
SC45
SR75
SR76
SR77
SR78

SR132
SR133

SR183
SC47
SC45

SR75
SR76
SR77
SR78

SR132
SR133

SR116
SR100
SR115
SR105
R37442
SR103
SR109
SR110

SR107
SR124
SR159
SR123
SR132

SR183
SC47
SC45
SR75
SR76
SR77
SR78

SR132
SR133

SR183
SC47
SC45

SR75
SR76
SR77
SR78

SR132
SR133

NOTE:
GPIO27 can be configured as wake input
to allow wakes from Deep Sleep.

NOTE:
External PU resistor required
if used for CLKREQ# functionality.

BMBUSY- (73)
LAN_DISABLE# (37)
SLP_LAN# (57,61)

LAN_CLK_REQ# (37)
LAN_DISABLE# (37)
SLP_LAN# (57,61)

SUS_WARN# (31)
SUS_ACK# (31)
SUS_CLK# (46,75)

LPC_PME# (74)
WAKE# (36,75)

SPKR (43)
SB_PWRBTN# (74)

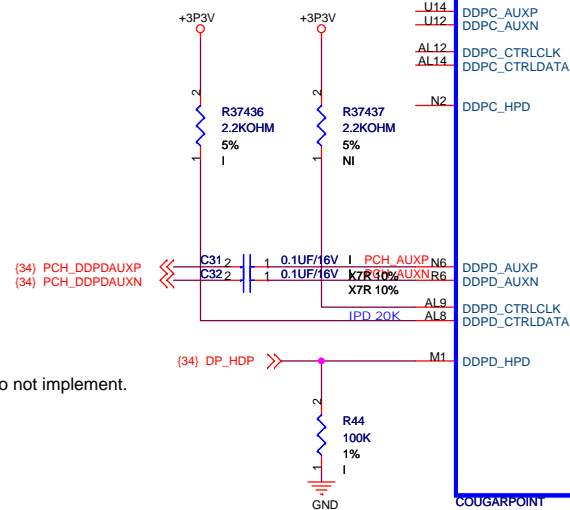
SLP_S3# (54,57,60,74)
SLP_S4# (53,54,57,58,74)
SLP_S5# (53,57,74)
SLP_A# (30,57,60,61)
SLP_SUS# (31,57,75)

SLP_S3#
SLP_S4#
SLP_S5#
SLP_A#
SLP_SUS#

NOTE:
SUSACK# and SUSWARN#
can be tied together if EC/SIO
does not want to involve in
the handshake mechanism
for the Deep Sleep entry and exit.

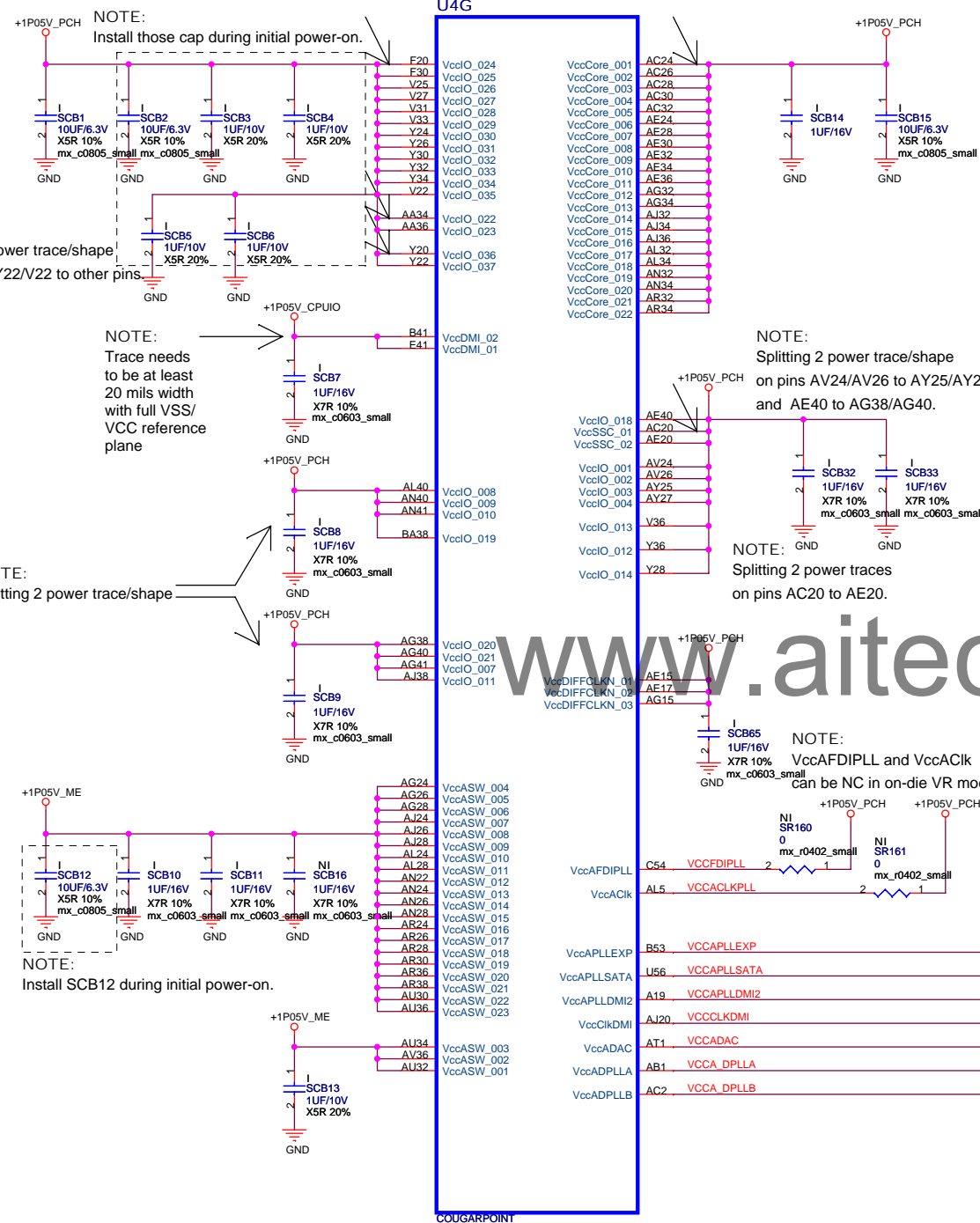
PIN	HIGH	LOW	DESCRIPTION
GPIO8	BTM	FCIM	Clock validation
GPIO15	Enable	Disable	TLS confidentiality
GPIO28	Enable	Disable	On-Die PLL VR

NOTE:
DDP[B..D]_HPD are 3.3V tolerant.

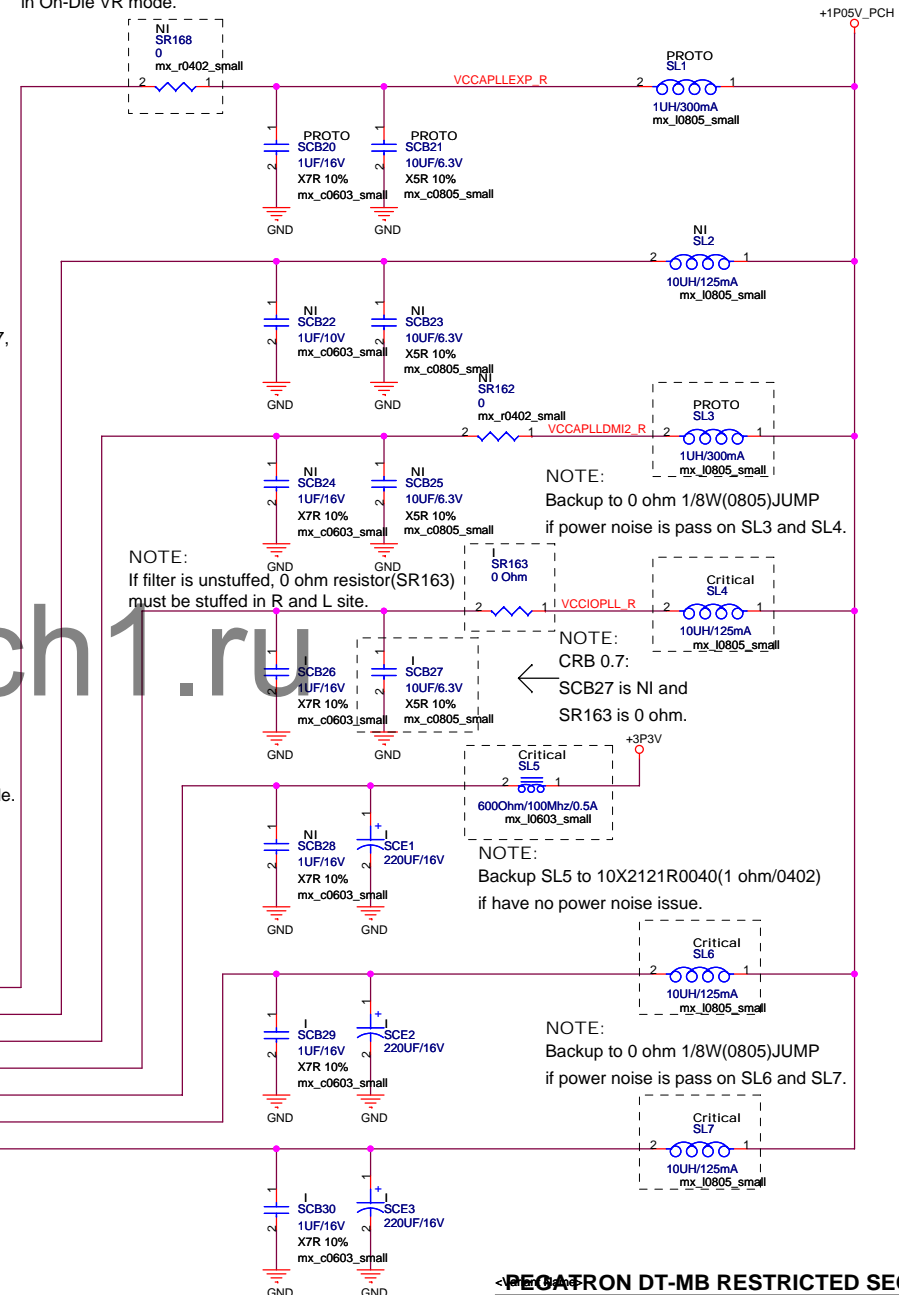


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Display Port



NOTE:
VccAPLLEXP, VccAPLLSATA, and VccAPLLDMI2 can be NC
in On-Die VR mode.



<Verbatim Name> **REGATRON DT-MB RESTRICTED SECRET**

PEGATRON Title : VCC/PLL 7-9

Pegatron Corp. Engineer: Scott Chen

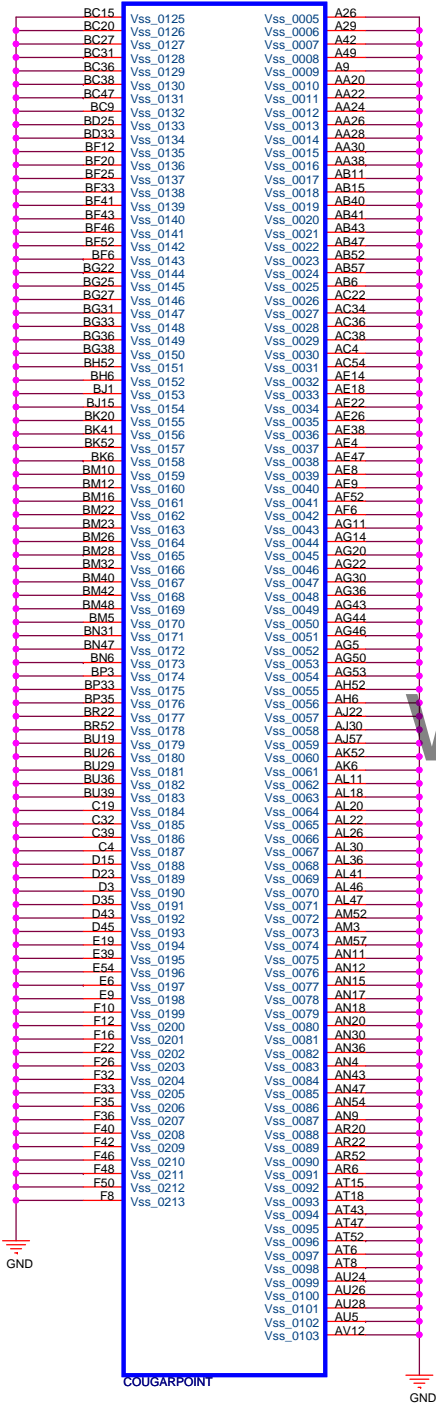
Size	Project Name	Rev
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A3	IPISB-SB	1.00
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Date: Thursday, April 14, 2011 Sheet 27 of 73

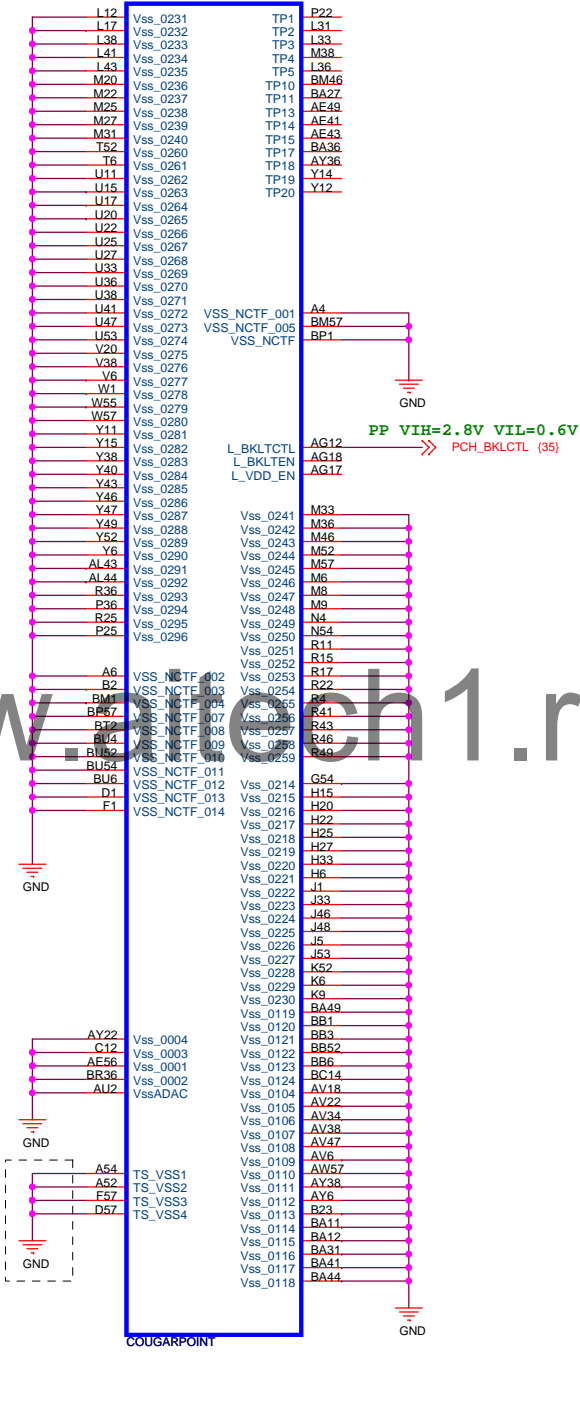
Critical

U4I



Critical

U4J



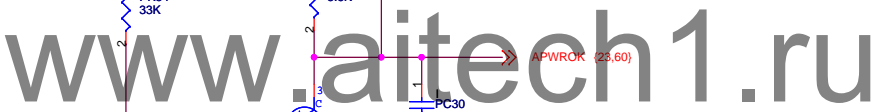
PEGATRON DT-MB RESTRICTED SECRET

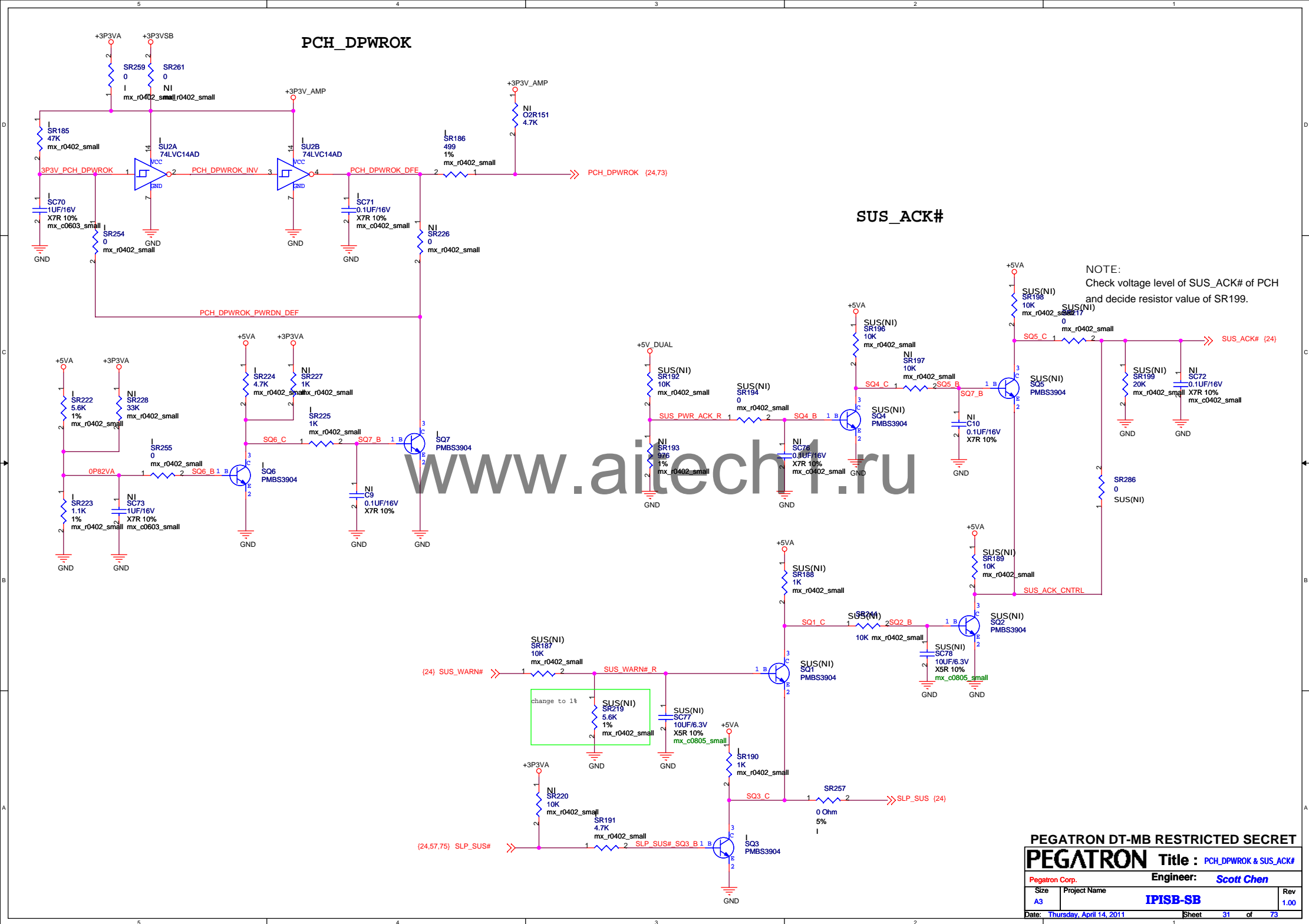
PEGATRON Title : VSS 9-9

Pegatron Corp. Engineer: Scott Chen

Size A3 Project Name IPISB-SB Rev 1.00

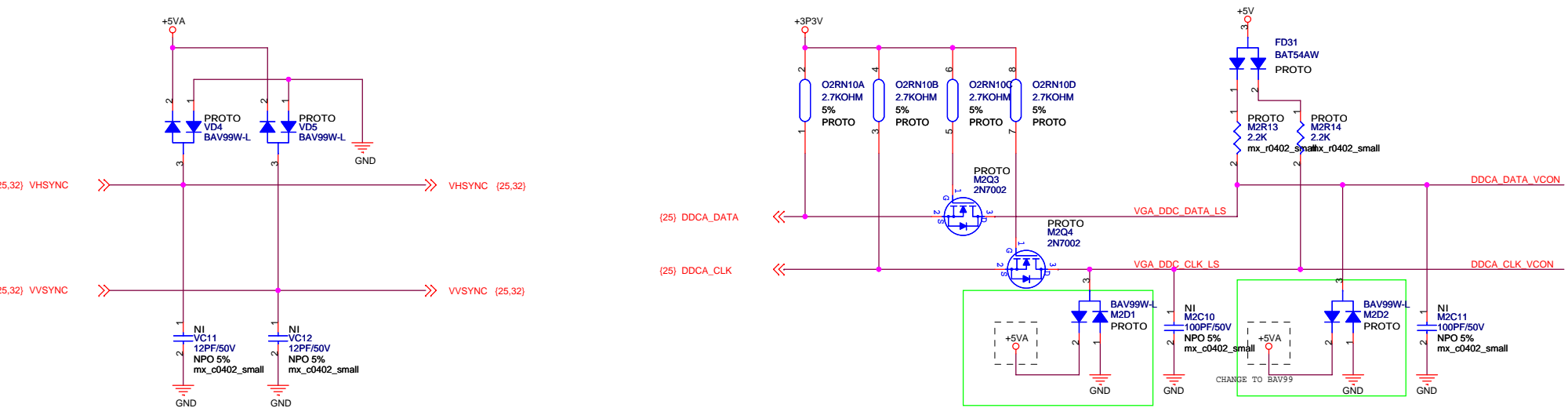
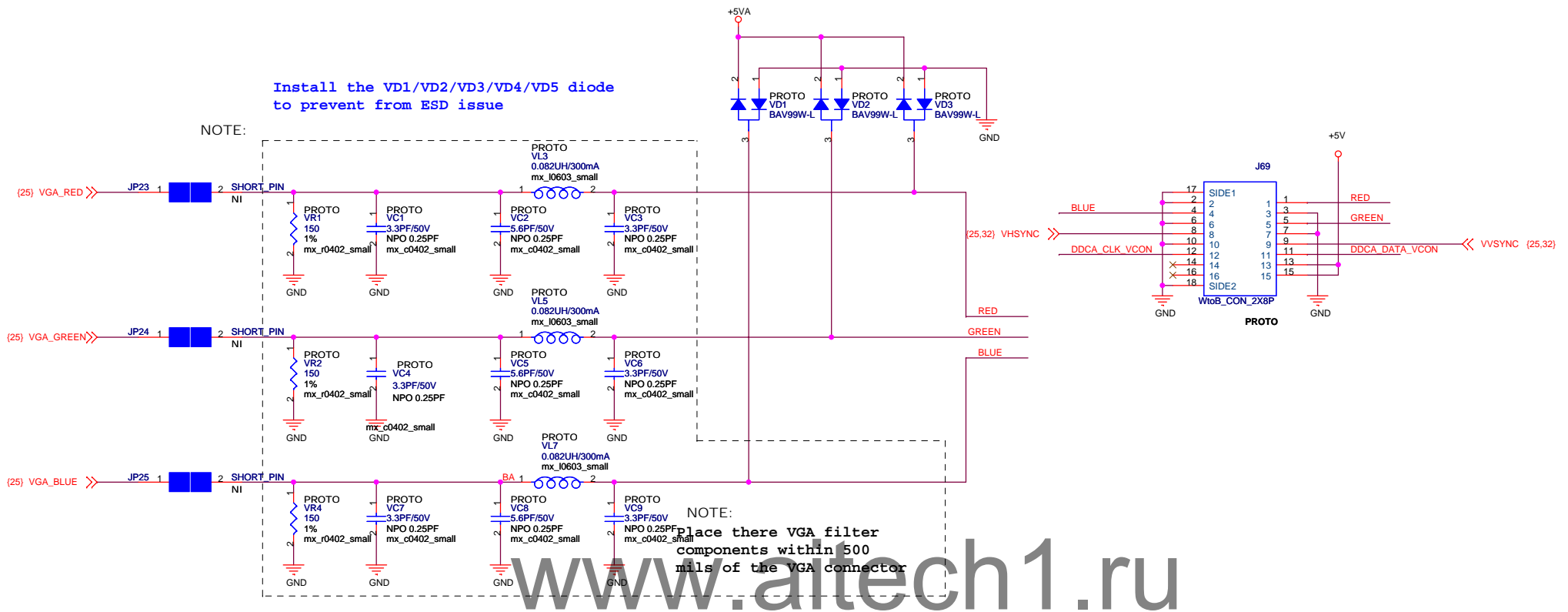
Date: Thursday, April 14, 2011 Sheet 29 of 73





Install the VD1/VD2/VD3/VD4/VD5 diode
to prevent from ESD issue

NOTE:



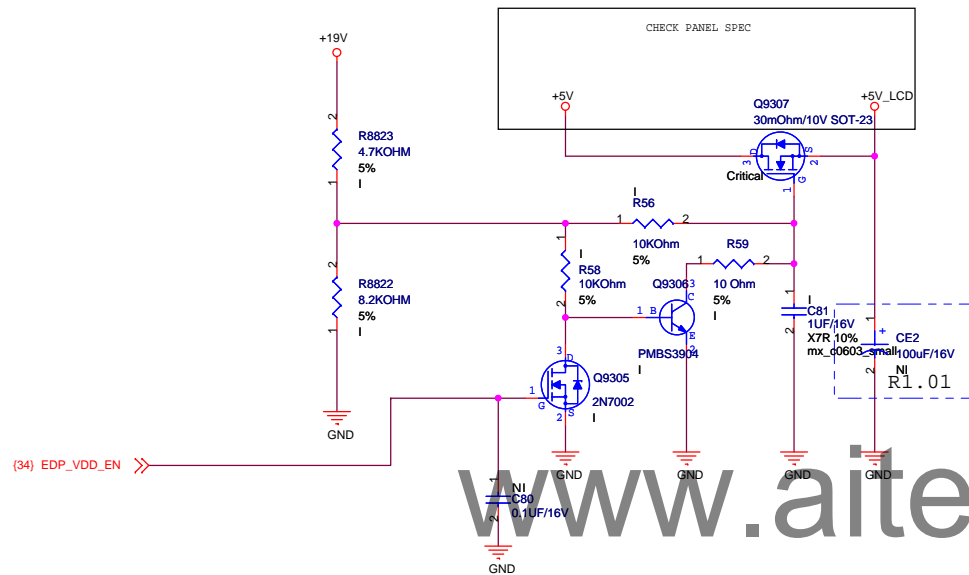
<Variant Name>

PEGATRON Title : **DEBUG VGA PORT**

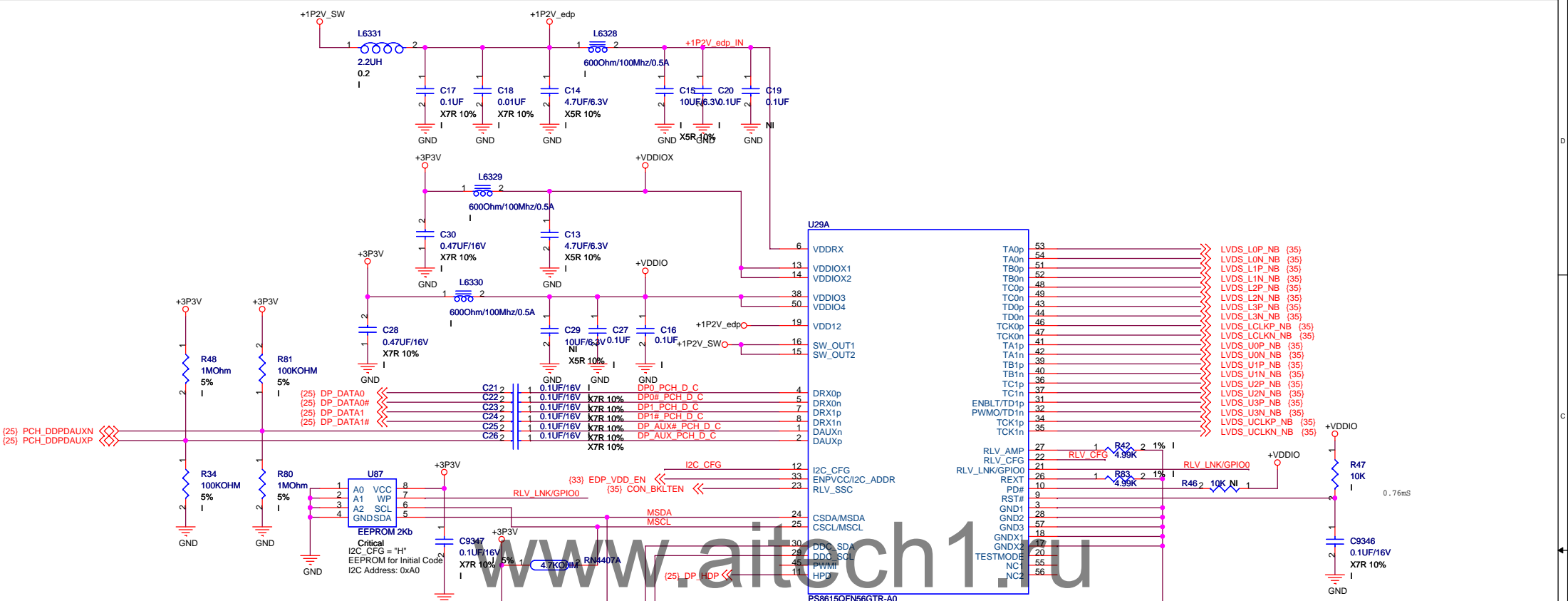
Pegatron Corp. Engineer: **Scott Chen**

Size	Project Name	Rev
A3	IPISB-SB	1.00

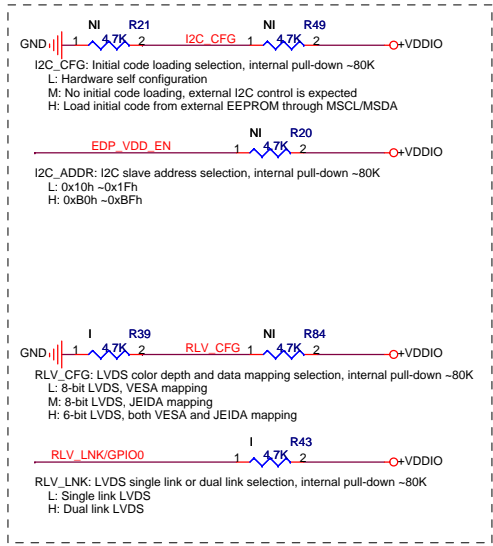
Date: Thursday, April 14, 2011 Sheet 32 of 73

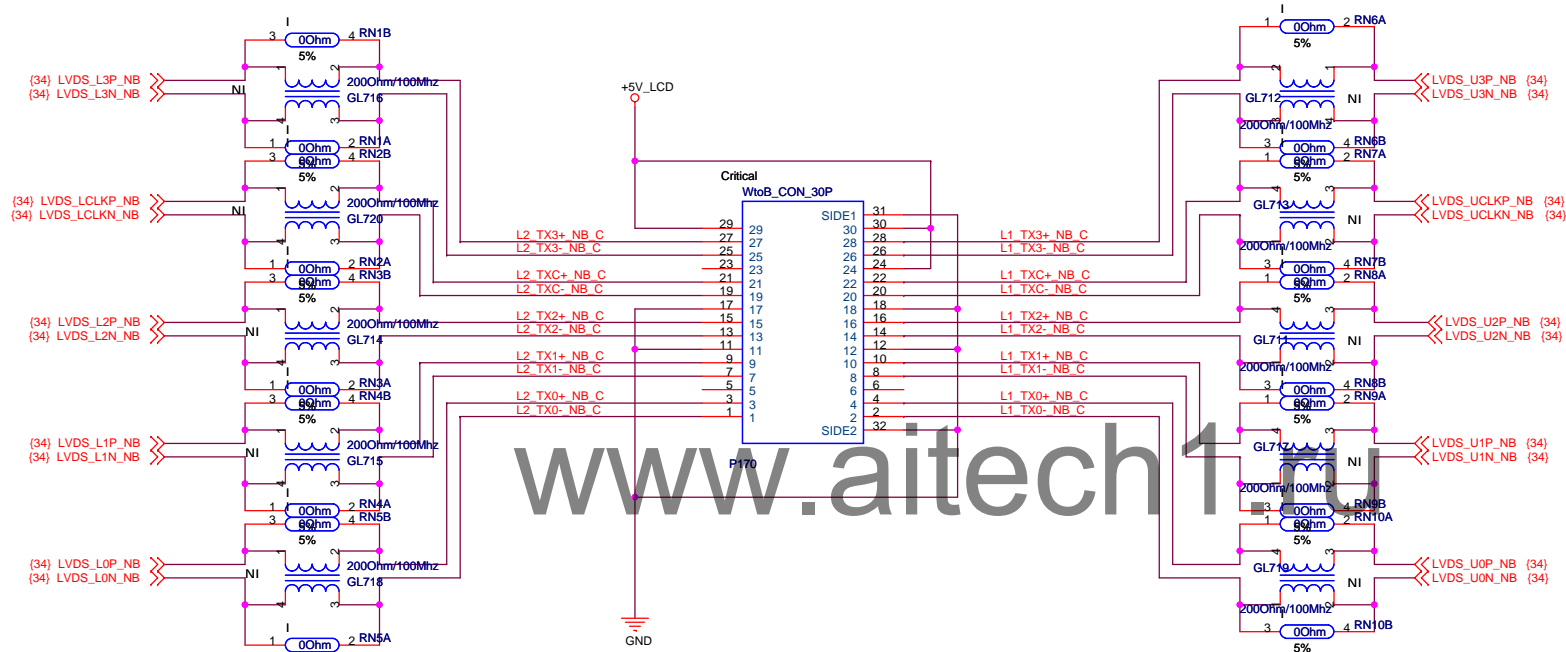


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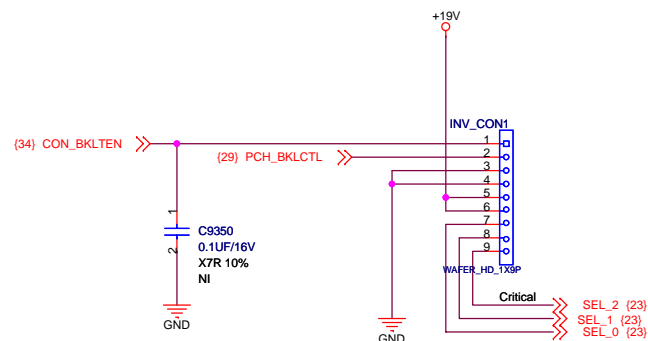
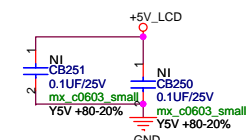


Power On Configuration

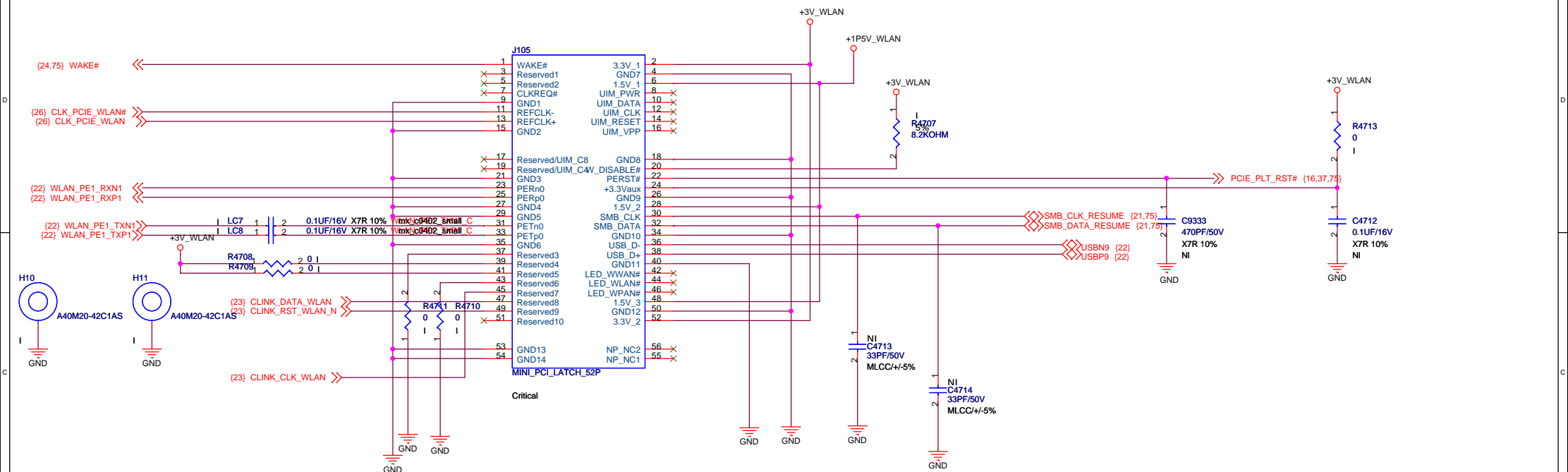




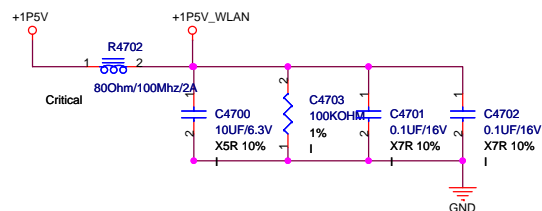
Inverter
Conn.



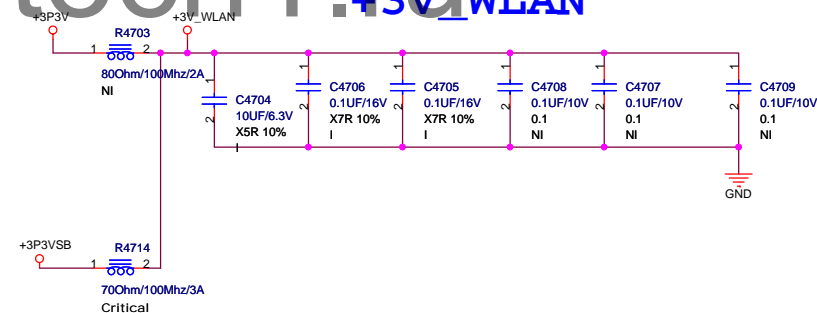
WLAN

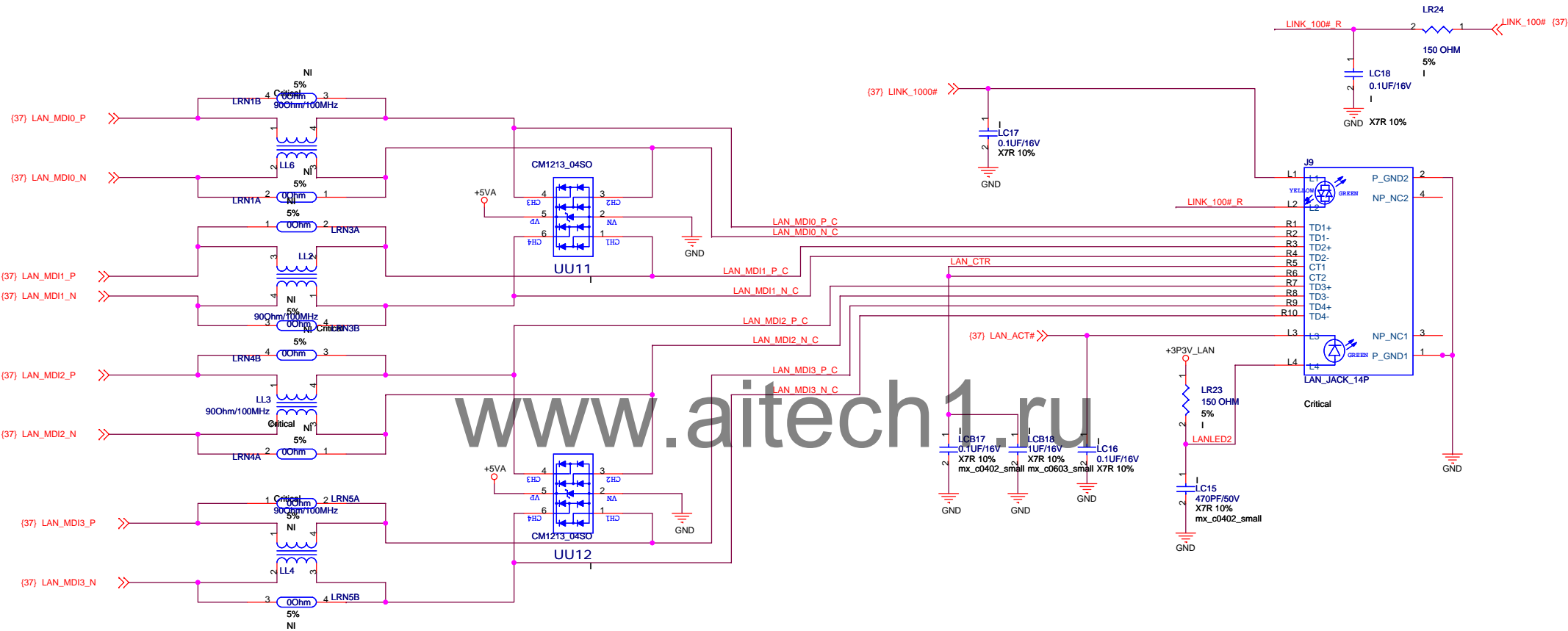


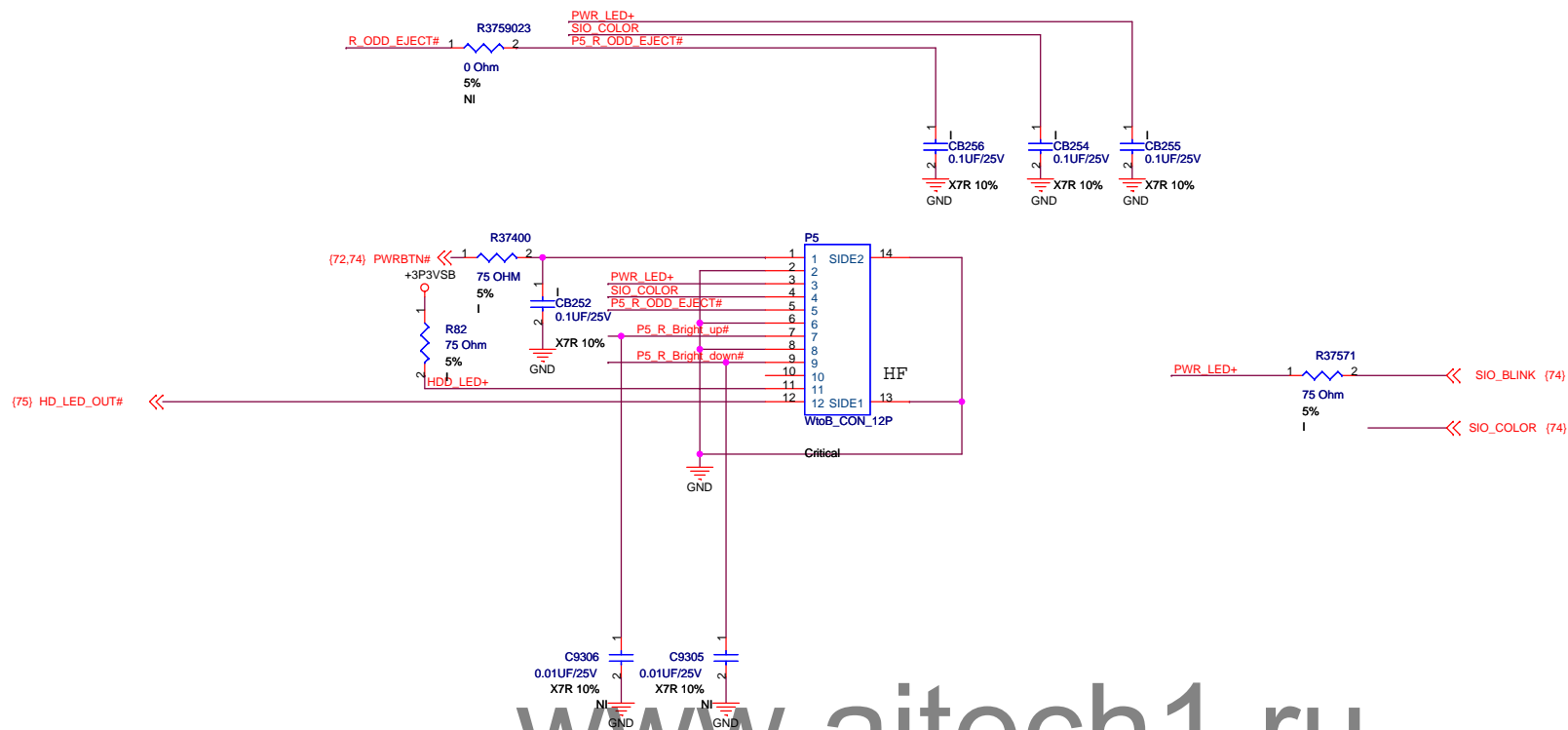
+1P5V_WLAN



+3V_WLAN

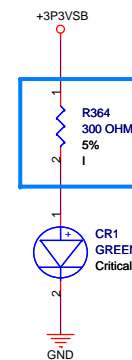






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Power supply LED



PEGATRON DT-MB RESTRICTED SECRET

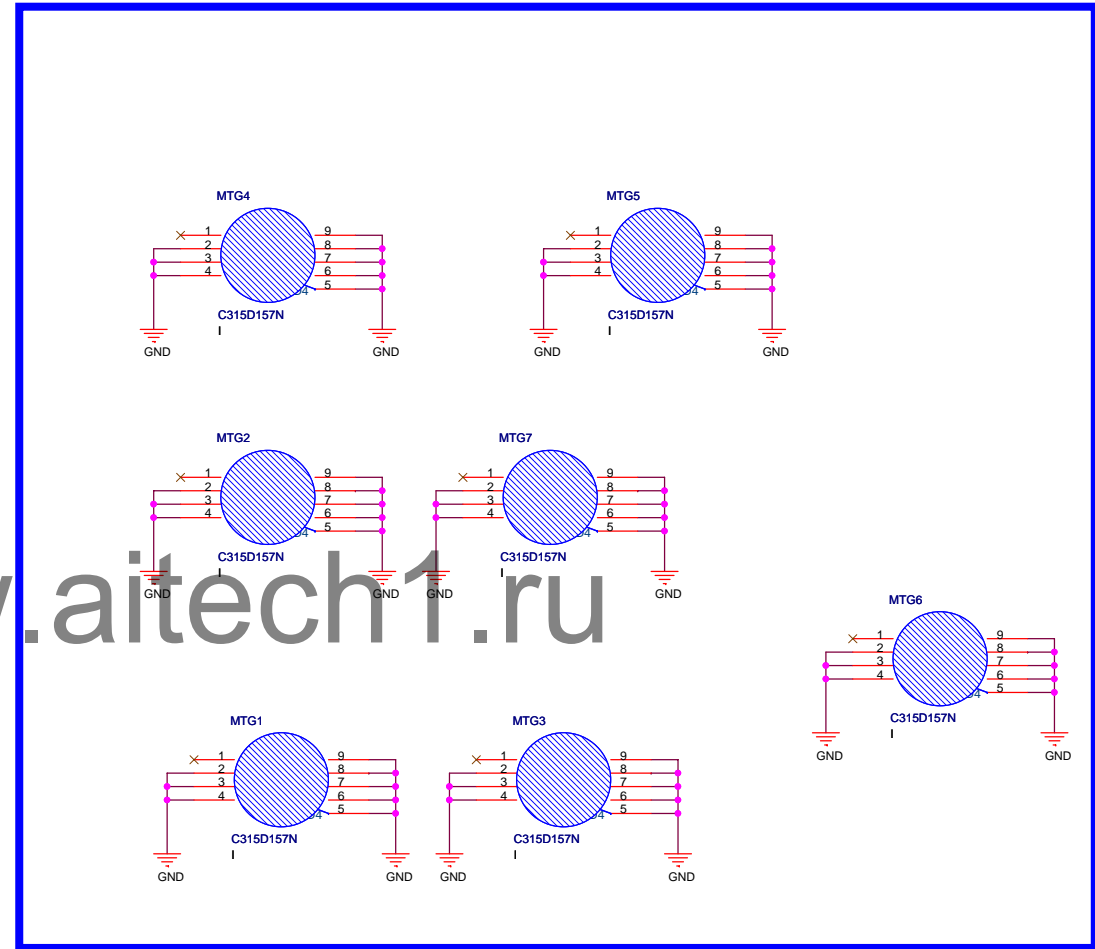
PEGATRON Title : FRONT PANEL

Pegatron Corp. Engineer: Scott Chen

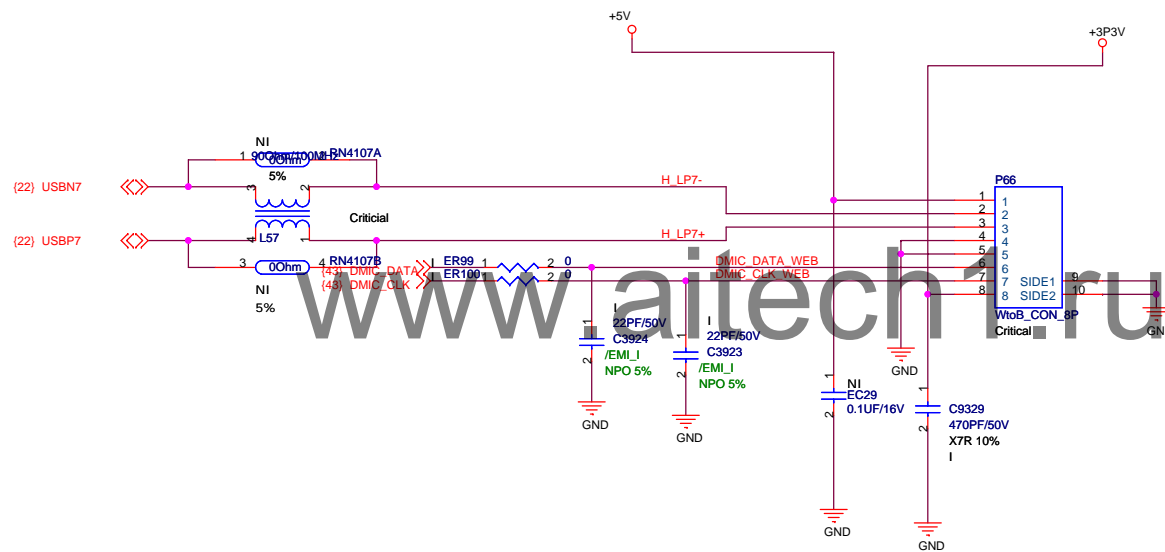
Size A3 Project Name IPISB-SB Rev 1.00

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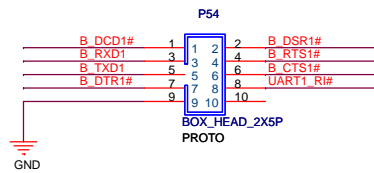
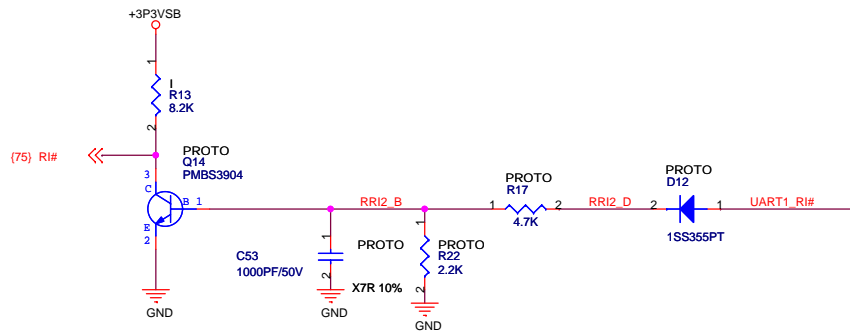
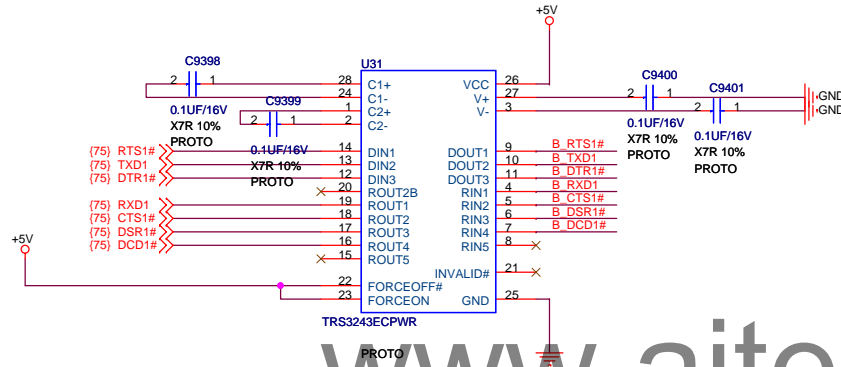
Critical
PCB2
IPISB-SB

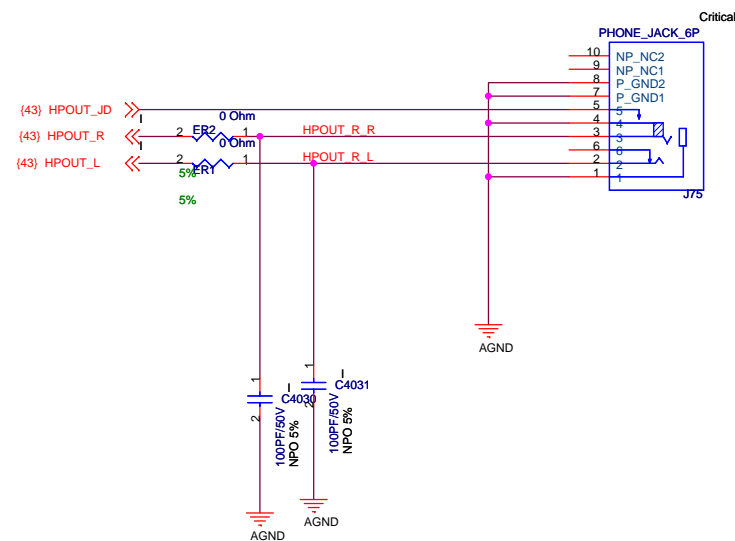
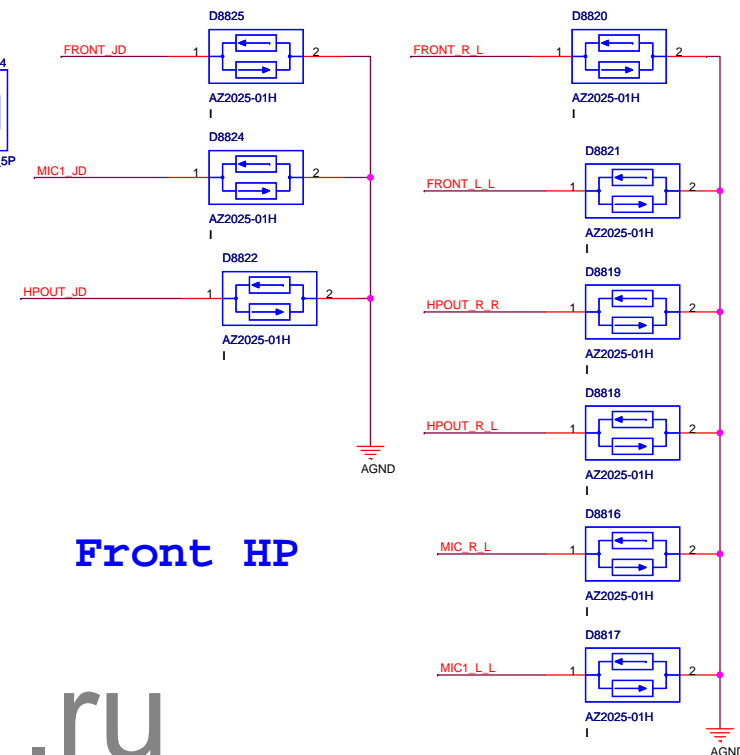


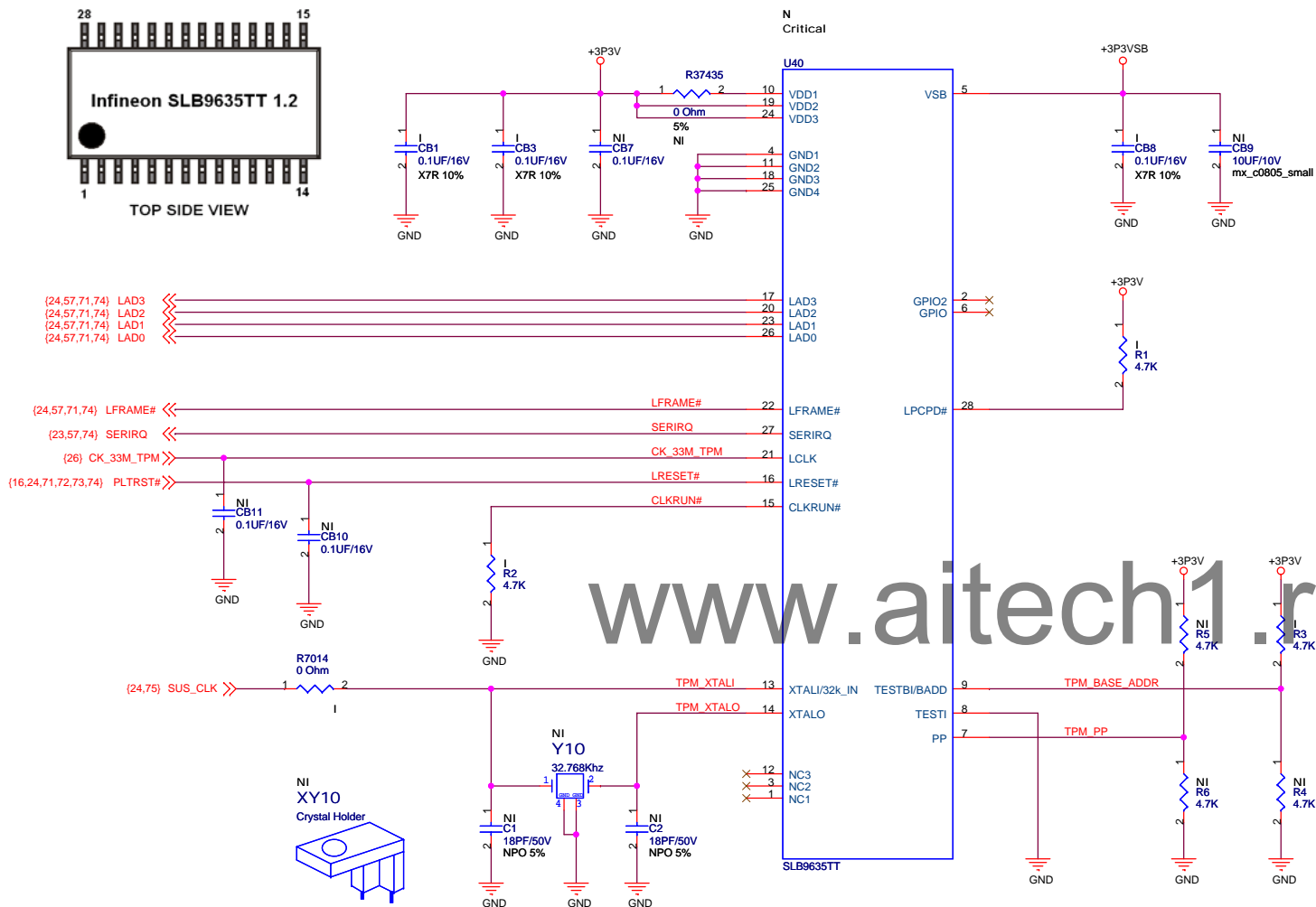
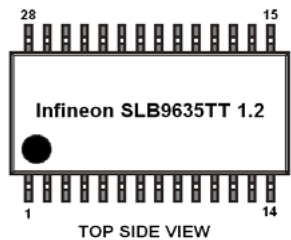
Webcam & Digital MIC CONNECTOR



COM HEADER





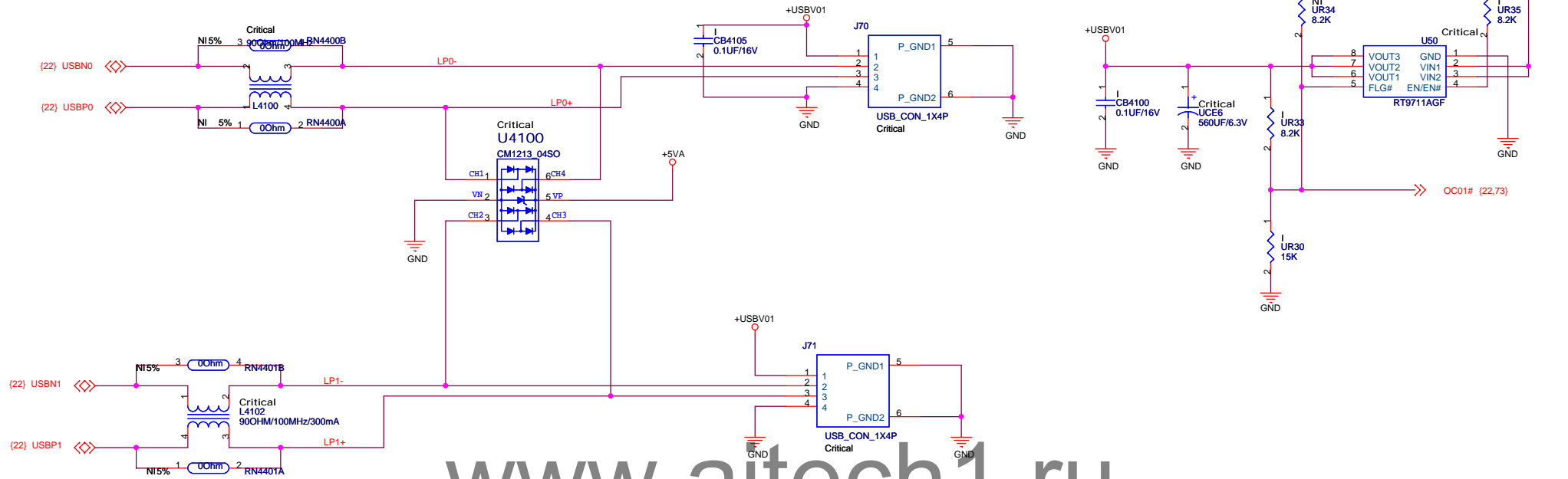


TPM_BASE_ADDR	I/O SPACE
0	2E
1	4E

<Variant Name>

PEGATRON		Title : TPM	
Pegatron Corp.		Engineer: Scott Chen	
Size A3	Project Name IPISB-SB	Rev 1.00	
Date: Thursday, April 14, 2011		Sheet 46 of 73	

Side USB



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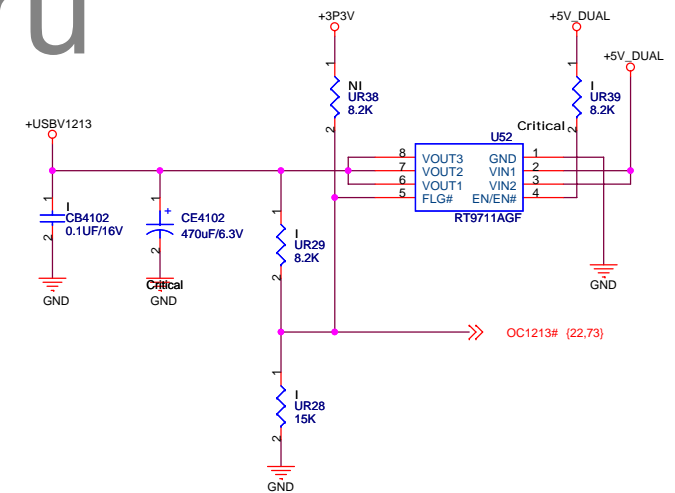
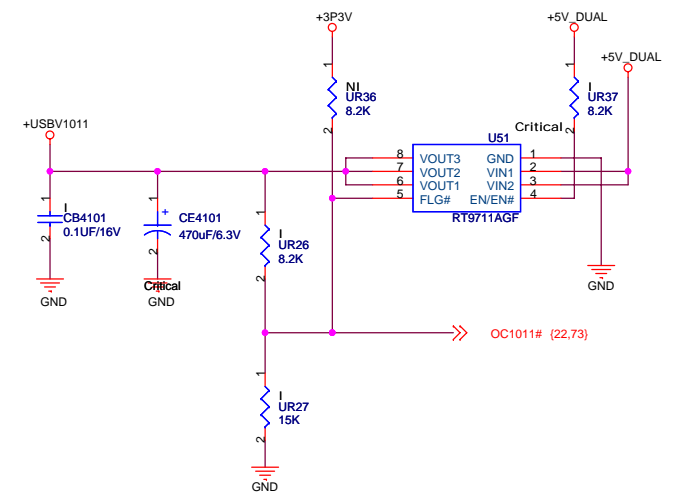
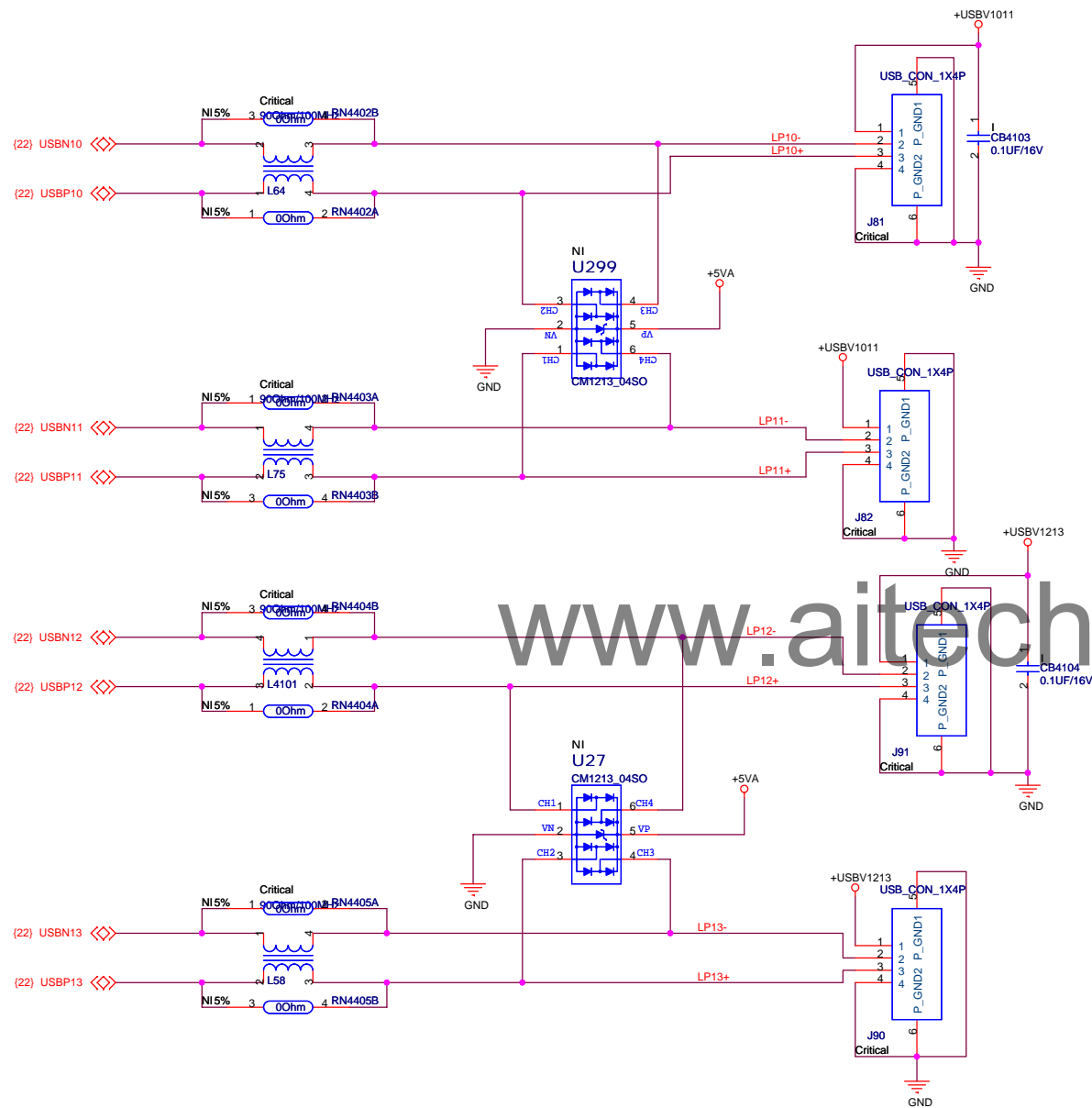
PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : SIDE USB

Pegatron Corp. Engineer: Scott Chen

Size A3	Project Name IPISB-SB	Rev 1.00
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SATA CONNECTOR

The schematic diagram illustrates the power supply section of the WAFER_HD_4 board. It features two main input rails: +5V and +12V. The +5V rail is connected to a 5V_HDD output and includes decoupling capacitors C328 (10uF/25V), C210 (22uF/6.3V), and C334 (0.1uF/16V). The +12V rail is connected to a 12V_HDD output and includes decoupling capacitors CE102 (100uF/16V), C339 (0.1uF/16V), and C348 (0.1uF/16V). Both rails are connected to a P160 connector labeled WAFER_HD_4, which is marked as 'Critical'.

(23) SATA_TXP1 << C460 2 1 0.01UF/25V X7R 10% SATA_TXP1 C

(23) SATA_TXN1 << C462 2 1 0.01UF/25V X7R 10% SATA_TXN1 C

(23) SATA_RXN1 << C464 2 1 0.01UF/25V X7R 10% SATA_RXN1 C

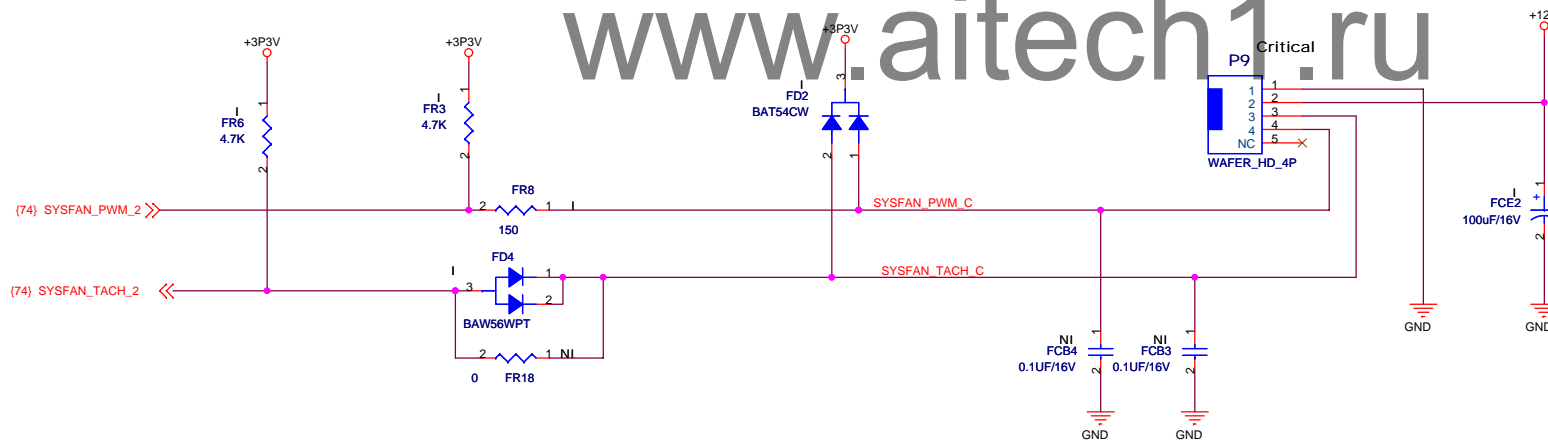
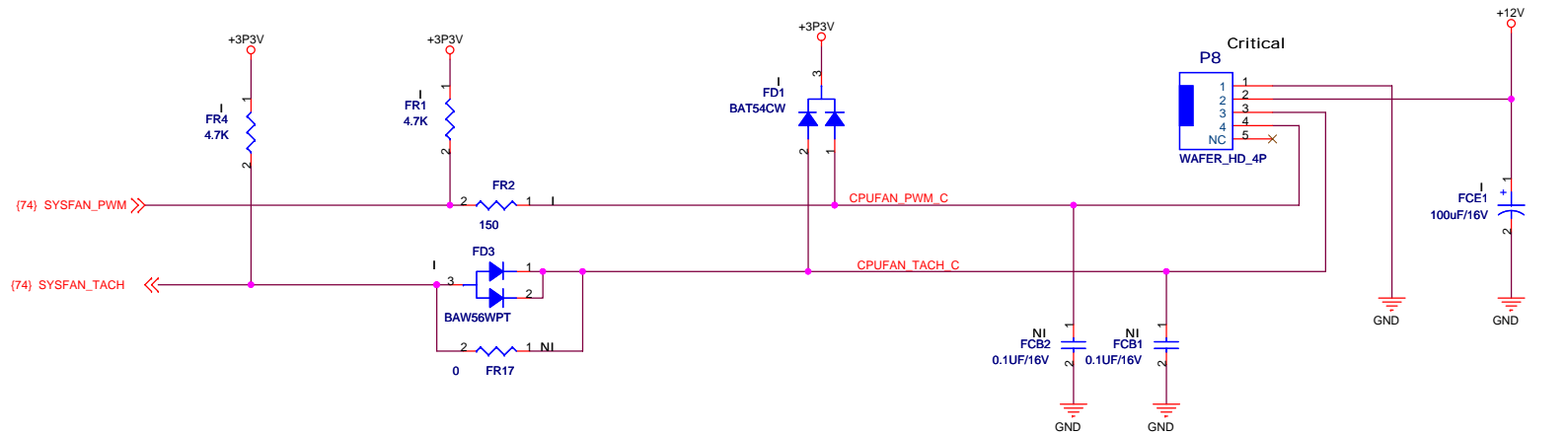
(23) SATA_RXP1 << C466 2 1 0.01UF/25V X7R 10% SATA_RXP1 C

GND

SATA_CON_7P

Critical

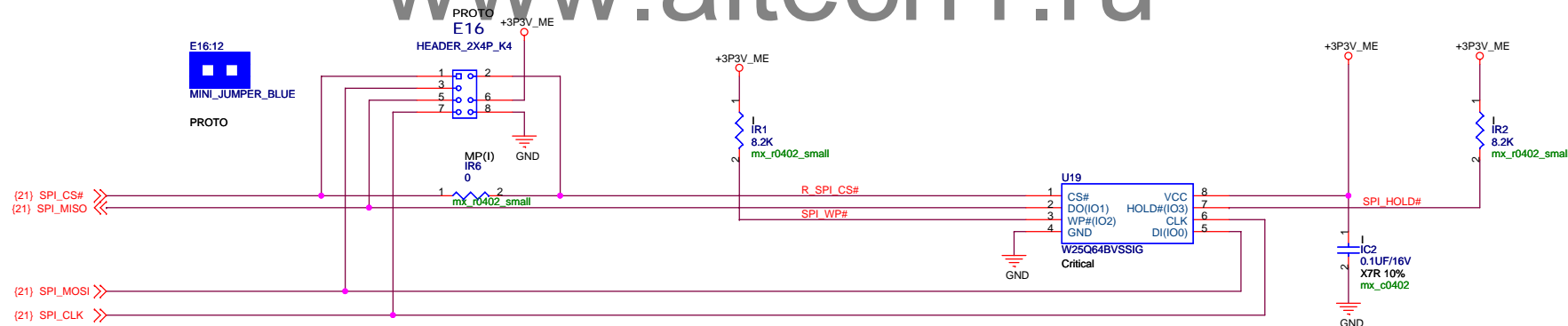
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<Variant Name>

PEGATRON		Title : SYSTEM FAN	
Pegatron Corp.		Engineer: Scott Chen	
Size	Project Name	Rev	
A3	IPISB-SB	1.00	
Date: Thursday, April 14, 2011		Sheet	50 of 73

SPI BIOS ROM - 64 Mbit

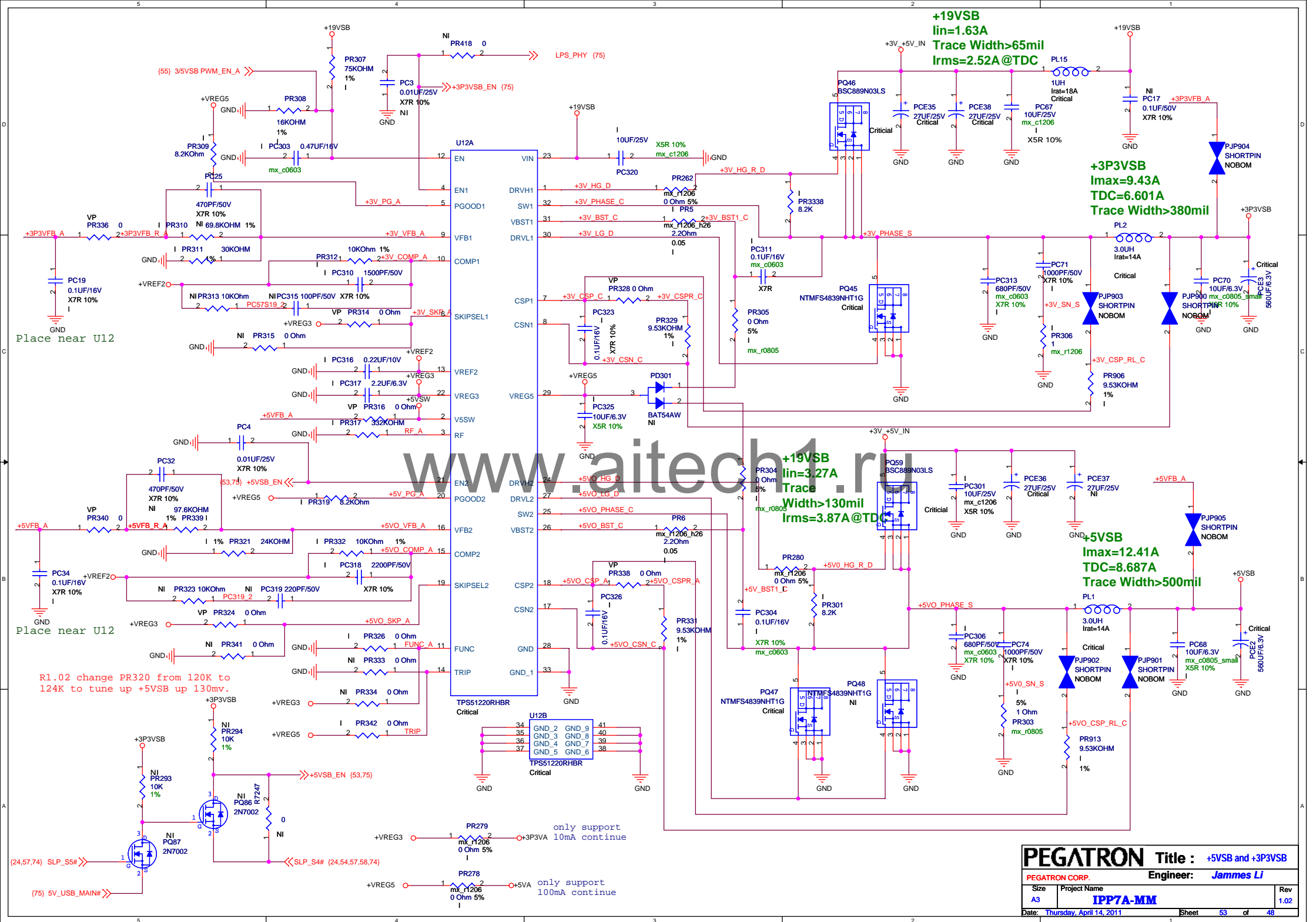


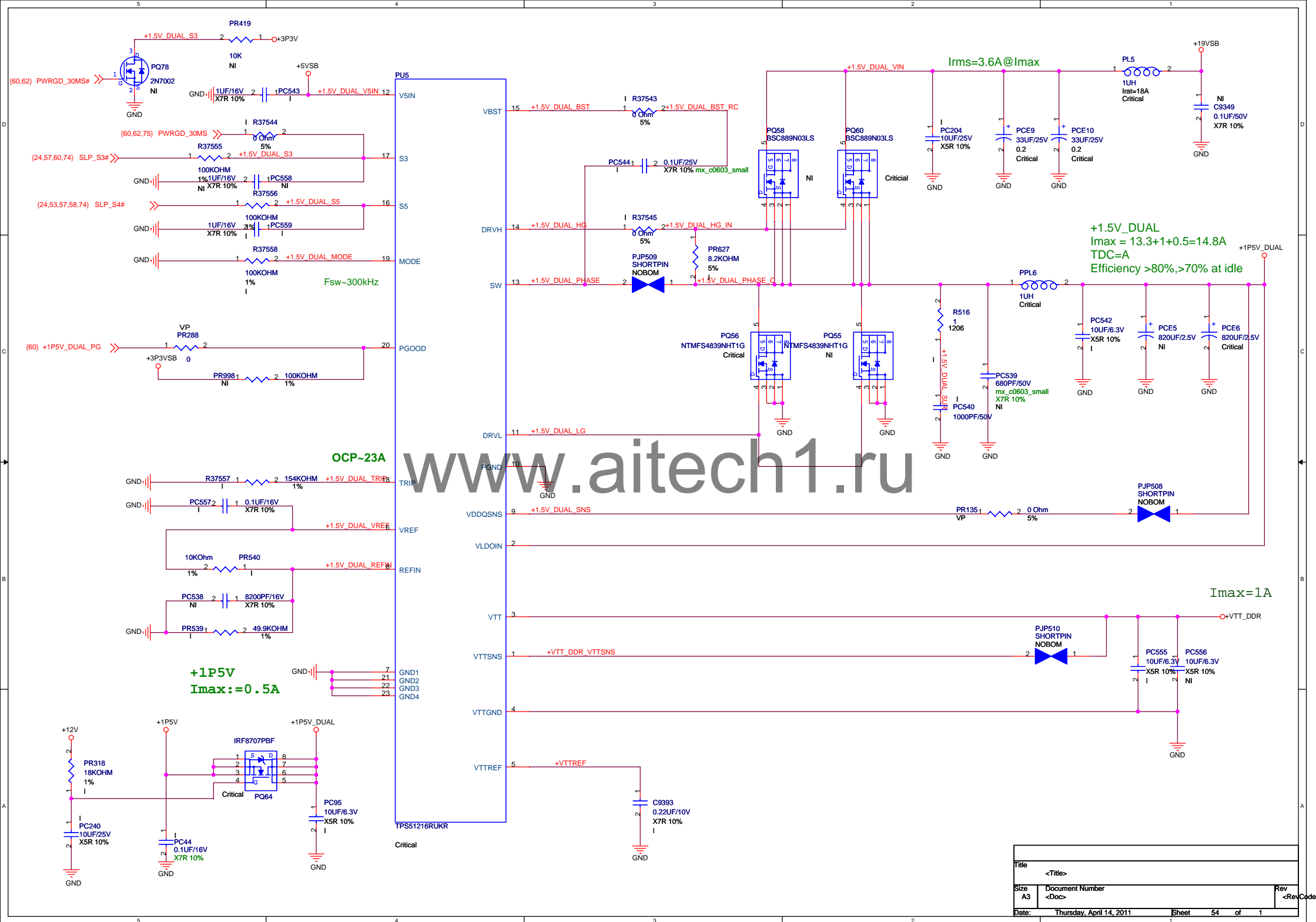
PEGATRON Title : SM BUS & SPI ROM

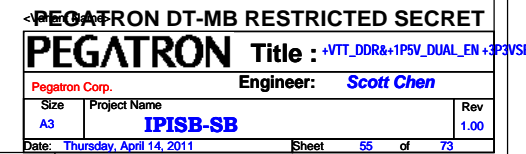
Size	Project Name	Rev
A3	IPISB-SB	1.00

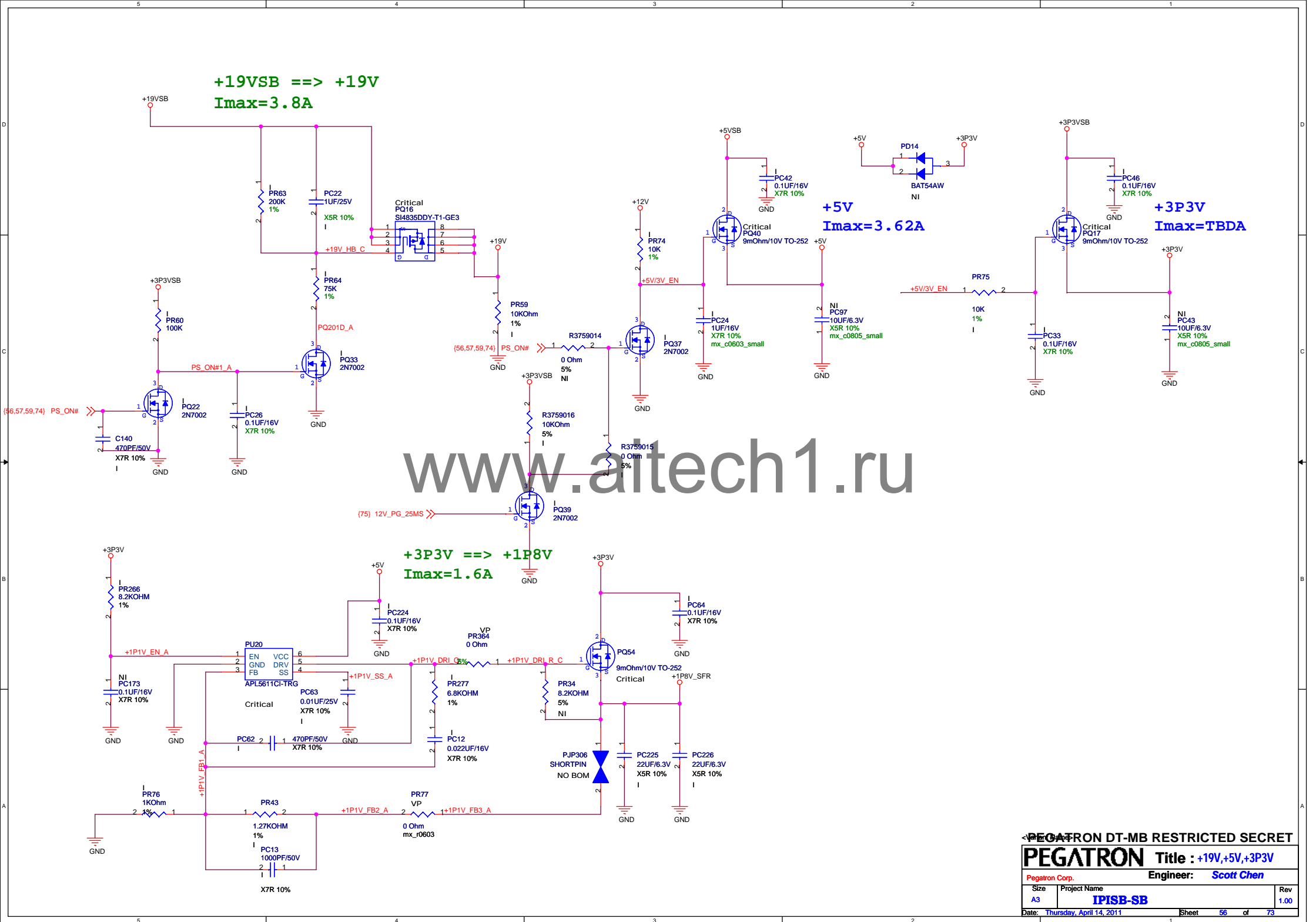
Date: Thursday, April 14, 2011 Sheet 51 of 73

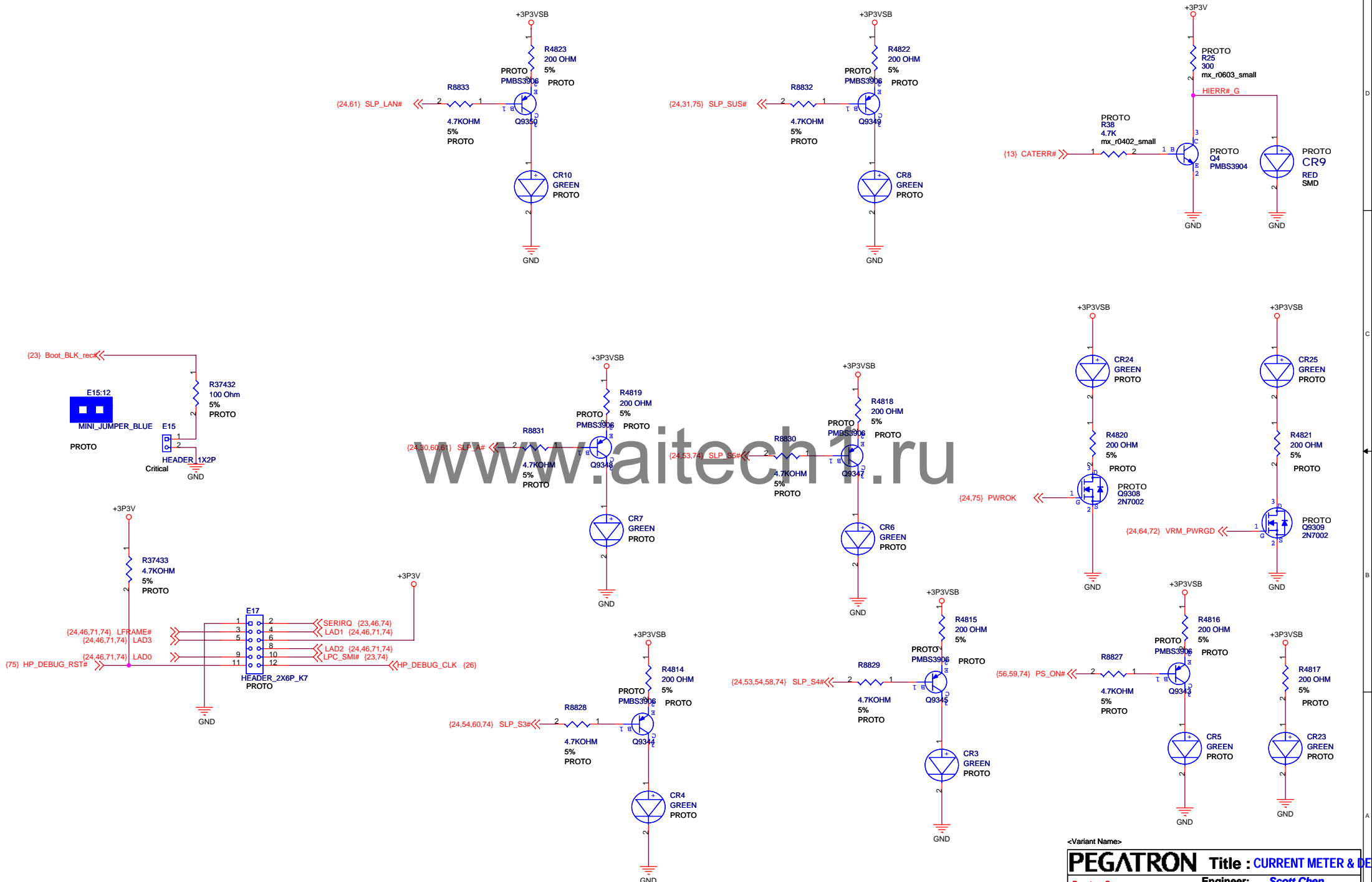


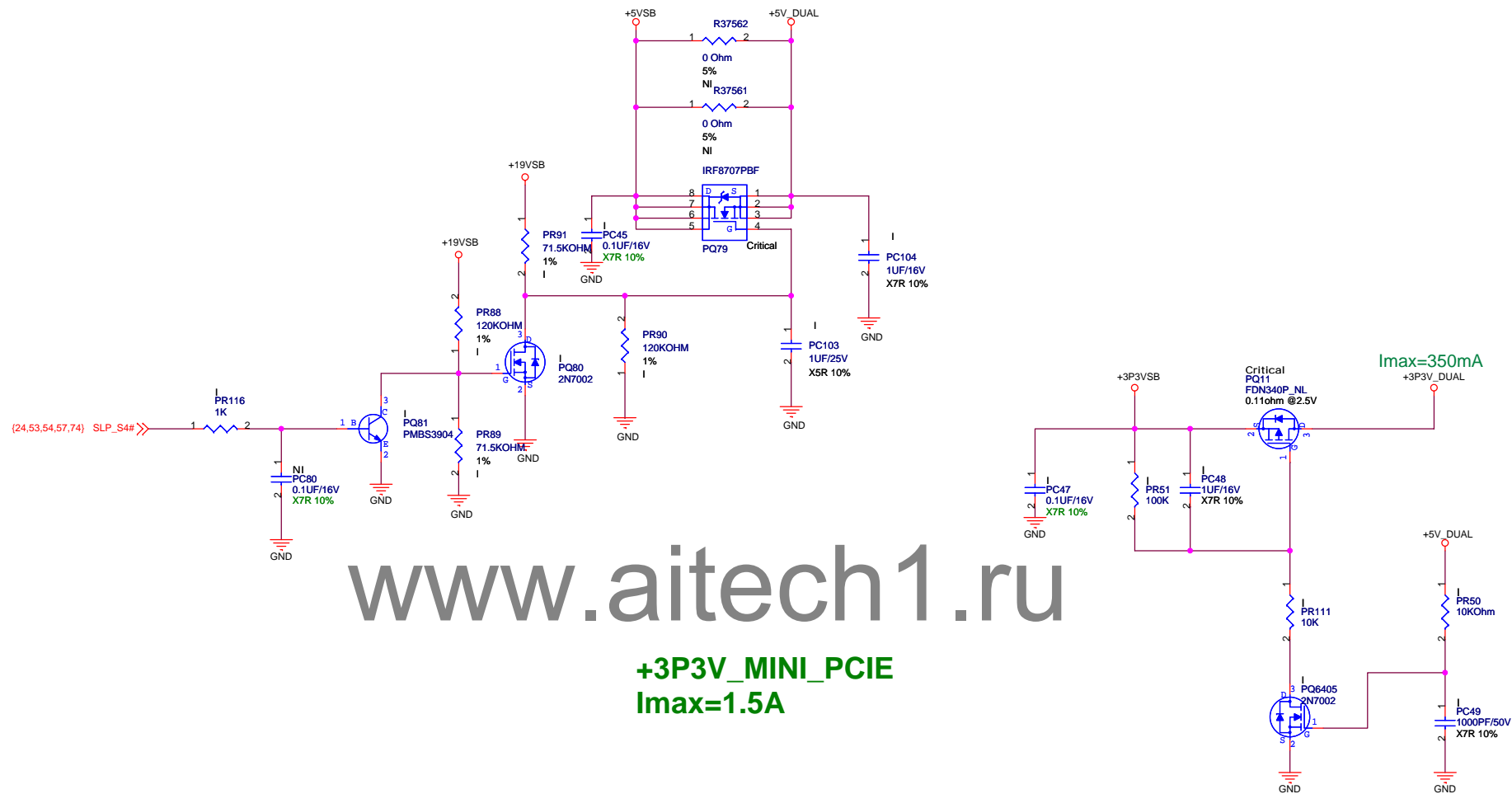










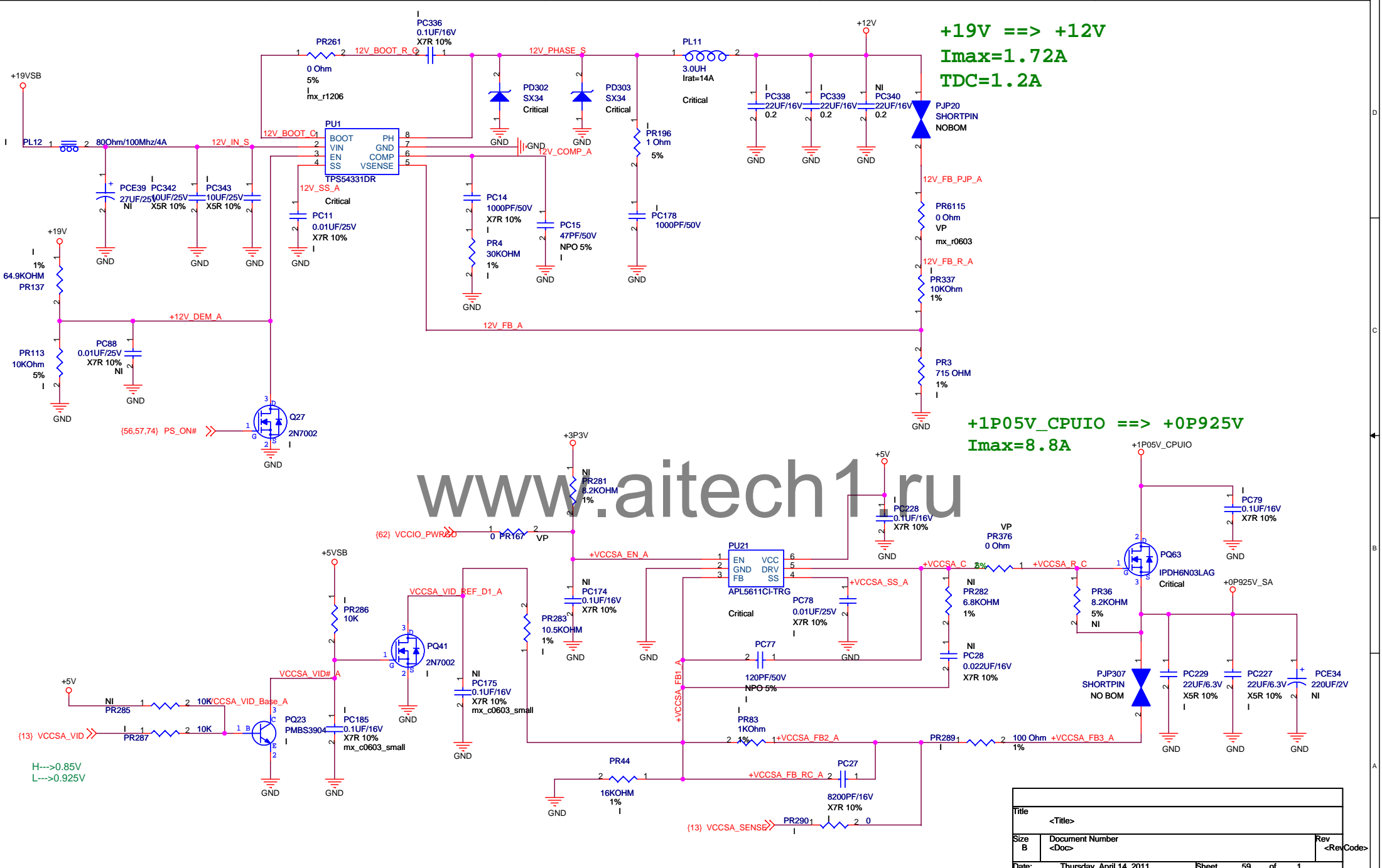


PEGATRON DT-MB RESTRICTED SECRET
<Variant Name>

PEGATRON Title : +5V_DUAL,+3P3V_DUAL

Pegatron Corp. Engineer: **Scott Chen**

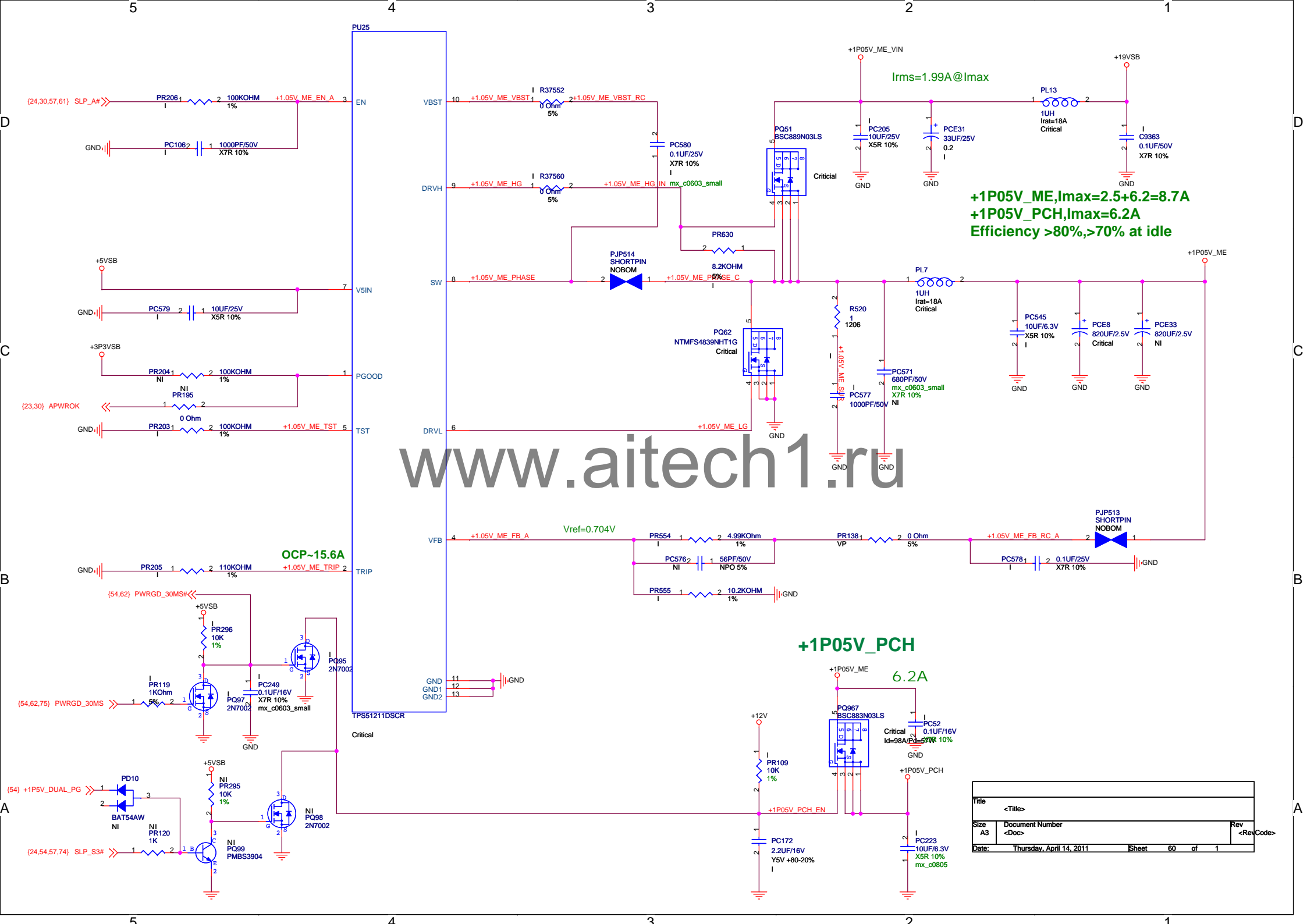
Size	Project Name	Rev
A3	IPISB-SB	1.00
Date: Thursday, April 14, 2011 Sheet 58 of 73		



+19V ==> +12V
Imax=1.72A
TDC=1.2A

+1P05V_CPUIO ==> +0P925V
Imax=8.8A

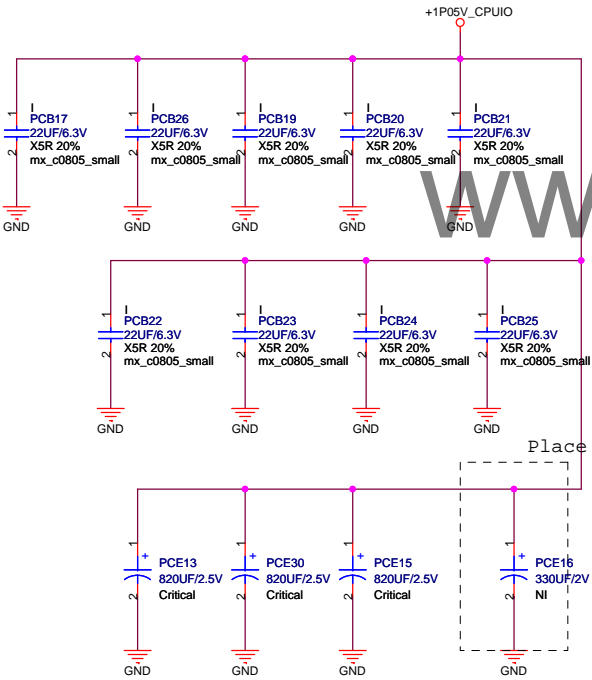
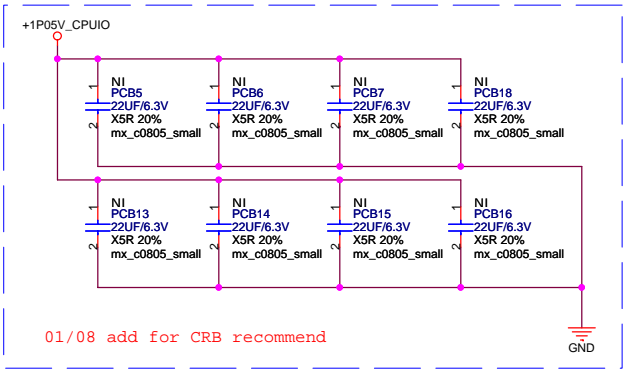
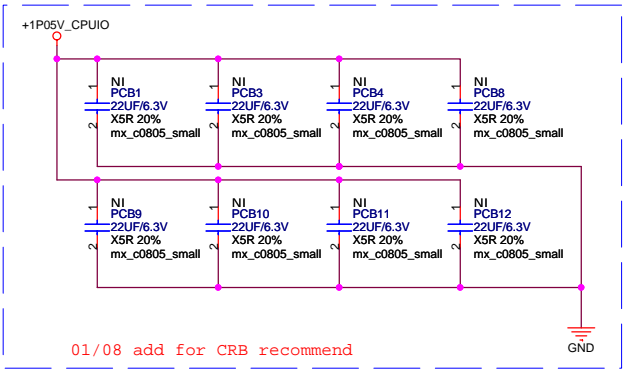
Title			<Title>
Size	Document Number	Rev	
B	<Doc>	<RevCode>	
Date:	Thursday, April 14, 2011	Sheet	59 of 1



Title			<Title>
Size	Document Number	Rev	
A3	<Doc>	<RevCode>	
Date:	Thursday, April 14, 2011	Sheet	60 of 1

VCCIO Decoupling Requirements

Capacitance	Qty	ESR (each)	ESL (each)	Filter	Placement	Notes
Aluminum Polymer 560μF	3	7mΩ	1.4nH	Output	Various. See layout figures	1
22μF 0805 X5R	9	5mΩ	0.55nH	Output	Inside processor socket cavity	1, 2 3
0805 placeholders	16				Backside	



Place close to CPU bottom side

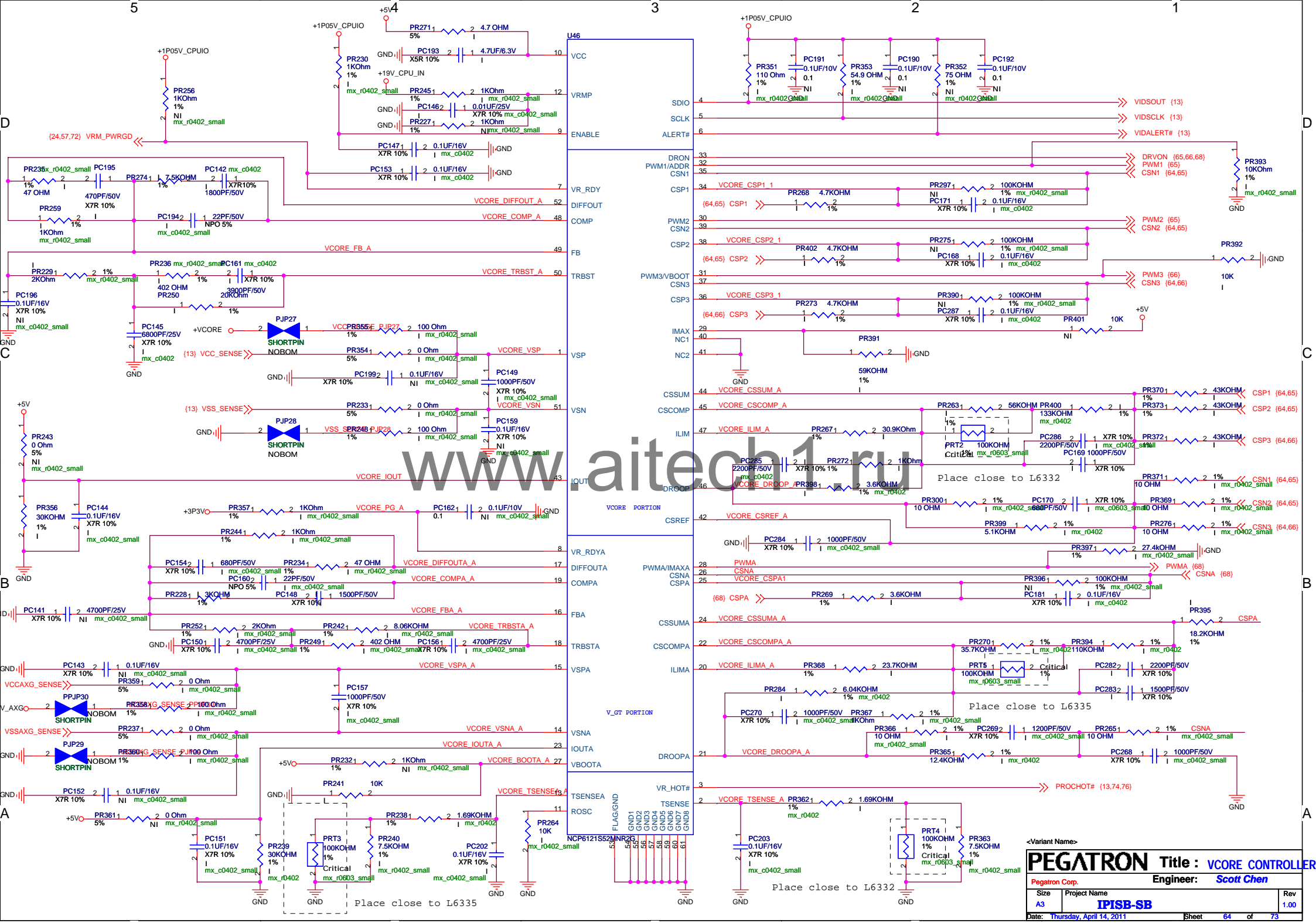
PEGATRON DT-MB RESTRICTED SECRET

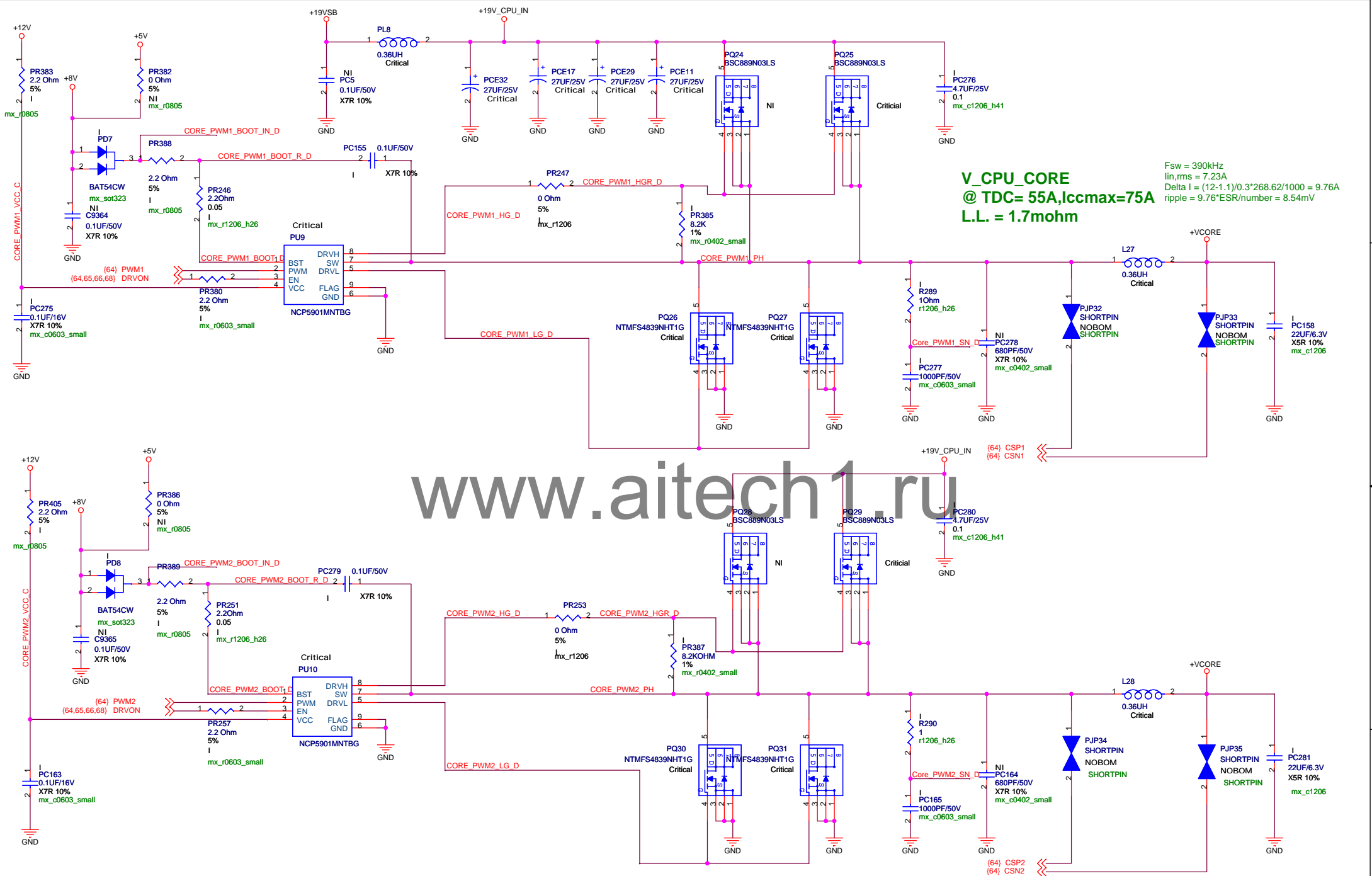
PEGATRON Title : +1P05V_CPUIO CAP

Pegatron Corp. Engineer: Scott Chen

Size A3 Project Name IPISB-SB Rev 1.00

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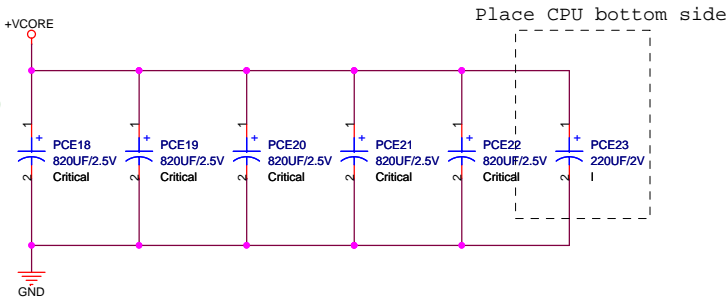
V_CPU_CORE
@ TDC= 55A, Iccmax=75A
L.L. = 1.7mohm

Fsw = 390kHz
Iin,rms = 7.23A
Delta I = (12-1.1)/0.3*268.62/1000 = 9.76A
ripple = 9.76*ESR/number = 8.54mV

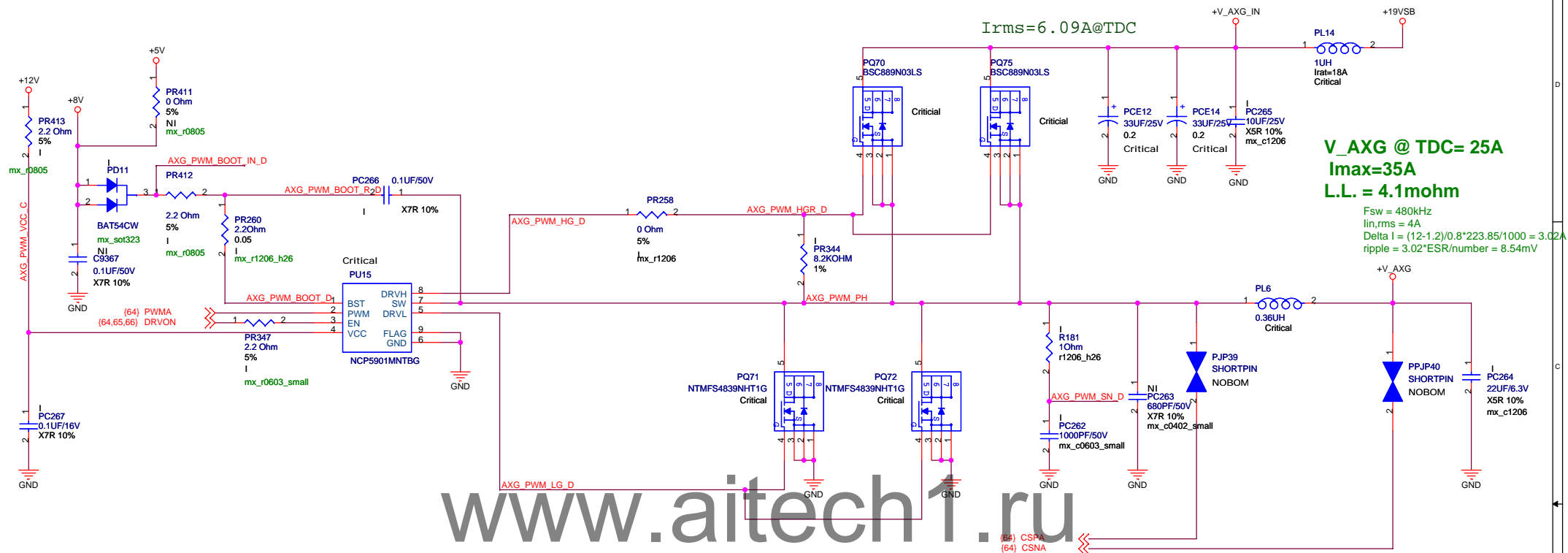
Table 30 Output CAP Requirements

Capacitance	Qty	ESR (each)	ESL (each)	Filter	Placement	Notes
Aluminum Polymer 560µF	4	7mΩ	1.4nH	Output	North of processor - as close to RM keep-out as possible	1
22µF 0805 X5R	18	5mΩ	0.55nH	Output	14 - Inside processor socket cavity 4- North of processor - as close to RM keep-out as possible	1, 2 3
Aluminum Electrolytic 390µF	4	51mΩ	6.1nH	Input		1
4.7µF X5R	9	7mΩ	0.6nH	Input		1

PL-CAP *4 +2(NI)
MLCC *18 +3(NI)



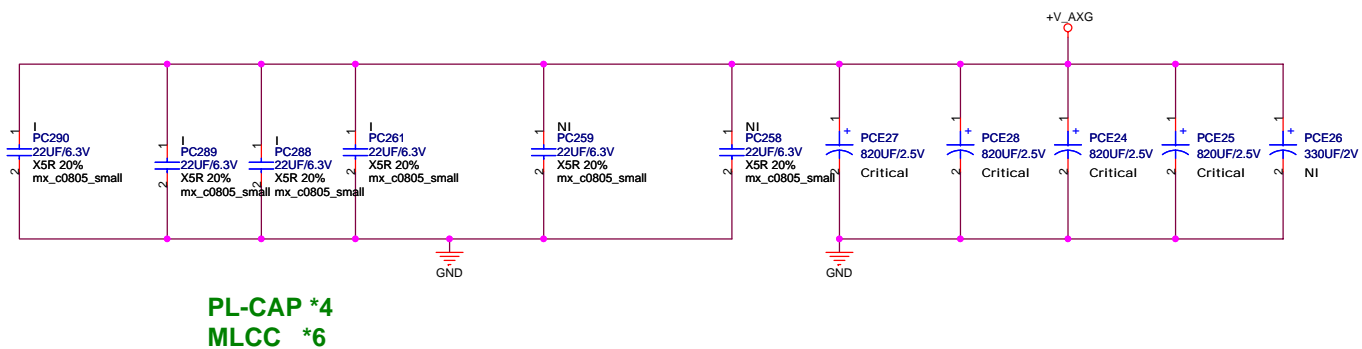
www.aitech1.ru



Output CAP

Table 30-4. VCCAXG Decoupling Requirements

Capacitance	Qty	ESR (each)	ESL (each)	Filter	Placement	Notes
Aluminum Polymer 560µF	4	7mΩ	1.4nH	Output	East of processor - as close to RM keep-out as possible	1
22µF 0805 X5R	6	5mΩ	0.55nH	Output	4 - inside processor socket cavity 2(empty) - Bottom of board, near socket	1, 2, 3
4.7µF X5R	3	7mΩ	0.6nH	Input		1

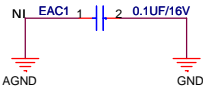
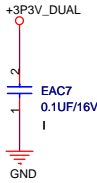
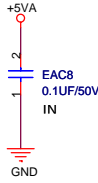
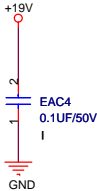
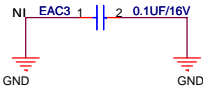
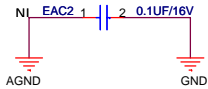
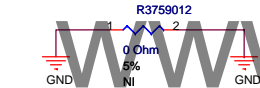
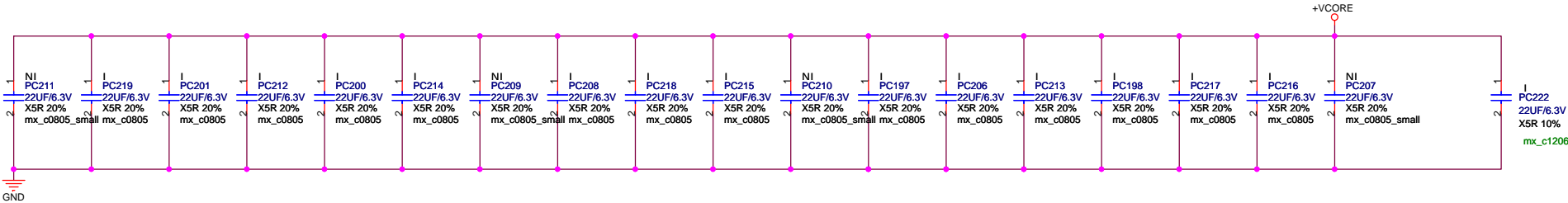


PEGATRON DT-MB RESTRICTED SECRET

PEGATRON		Title : +V_AXG DRIVER	
Pegatron Corp.		Engineer: Scott Chen	
Size	Project Name	Rev	
A3	IPISB-SB	1.00	
Date: Thursday, April 14, 2011		Sheet 68 of 73	

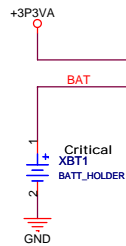
Output CAP Requirements

Capacitance	Qty	ESR (each)	ESL (each)	Filter	Placement	Notes
Aluminum Polymer 560µF	4	7mΩ	1.4nH	Output	North of processor - as close to RM keep-out as possible	1
22µF 0805 X5R	18	5mΩ	0.55nH	Output	14 - Inside processor socket cavity 4- North of processor - as close to RM keep-out as possible	1, 2 3
Aluminum Electrolytic 390µF	4	51mΩ	6.1nH	Input		1
4.7µF X5R	9	7mΩ	0.6nH	Input		1



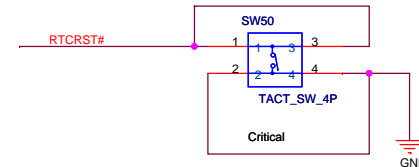
External RTC Circuitry

Critical
BATT1
3V/220mAh

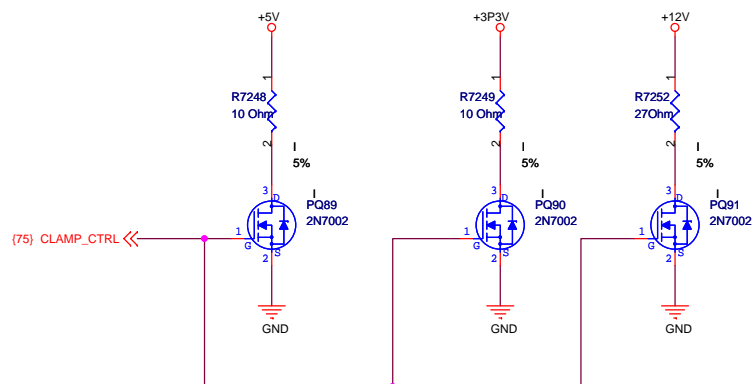


Battery Socket

NOTE:
Place C6 near PCH.



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PEGATRON DT-MB RESTRICTED SECRET

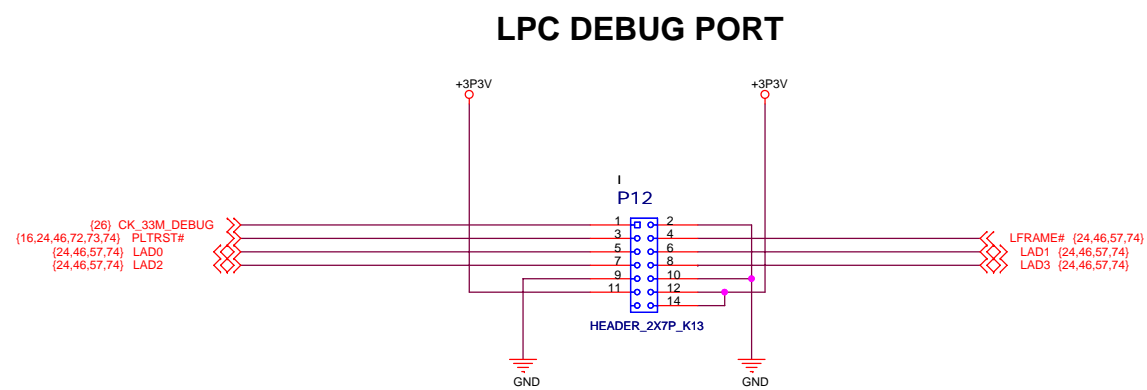
PEGATRON Title : RTC/CMOS/SPKR

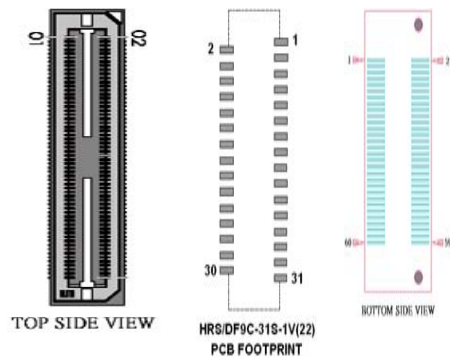
Pegatron Corp. Engineer: **Scott Chen**

Size A3	Project Name IPISB-SB	Rev 1.00
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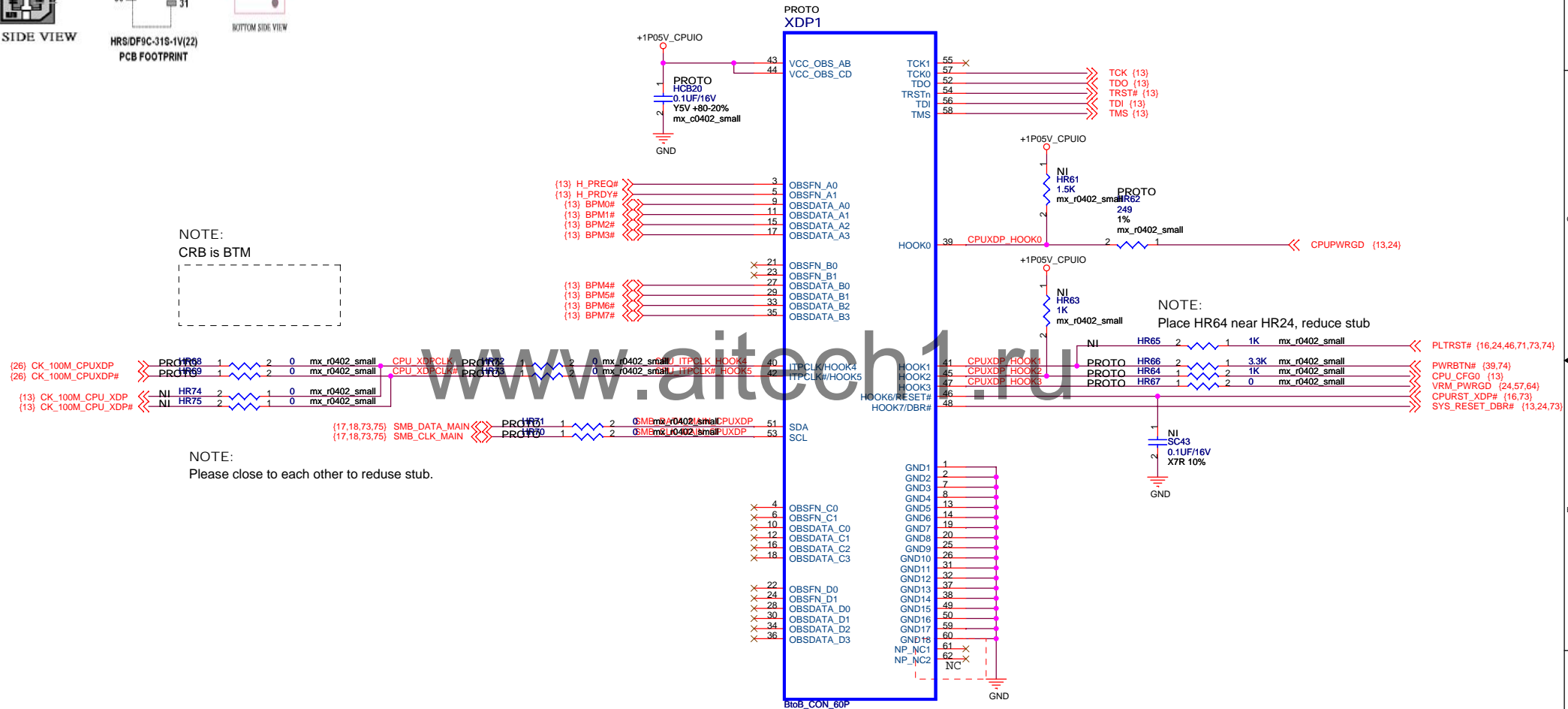
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INTEL CPU XDP DEBUG PORT



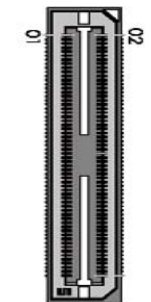
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PEGATRON Title : CPU XDP DEBUG

Engineer: *Scott Chen*

Size	Project Name	Rev
A3	IPISB-SB	1.00

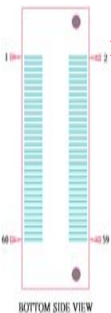
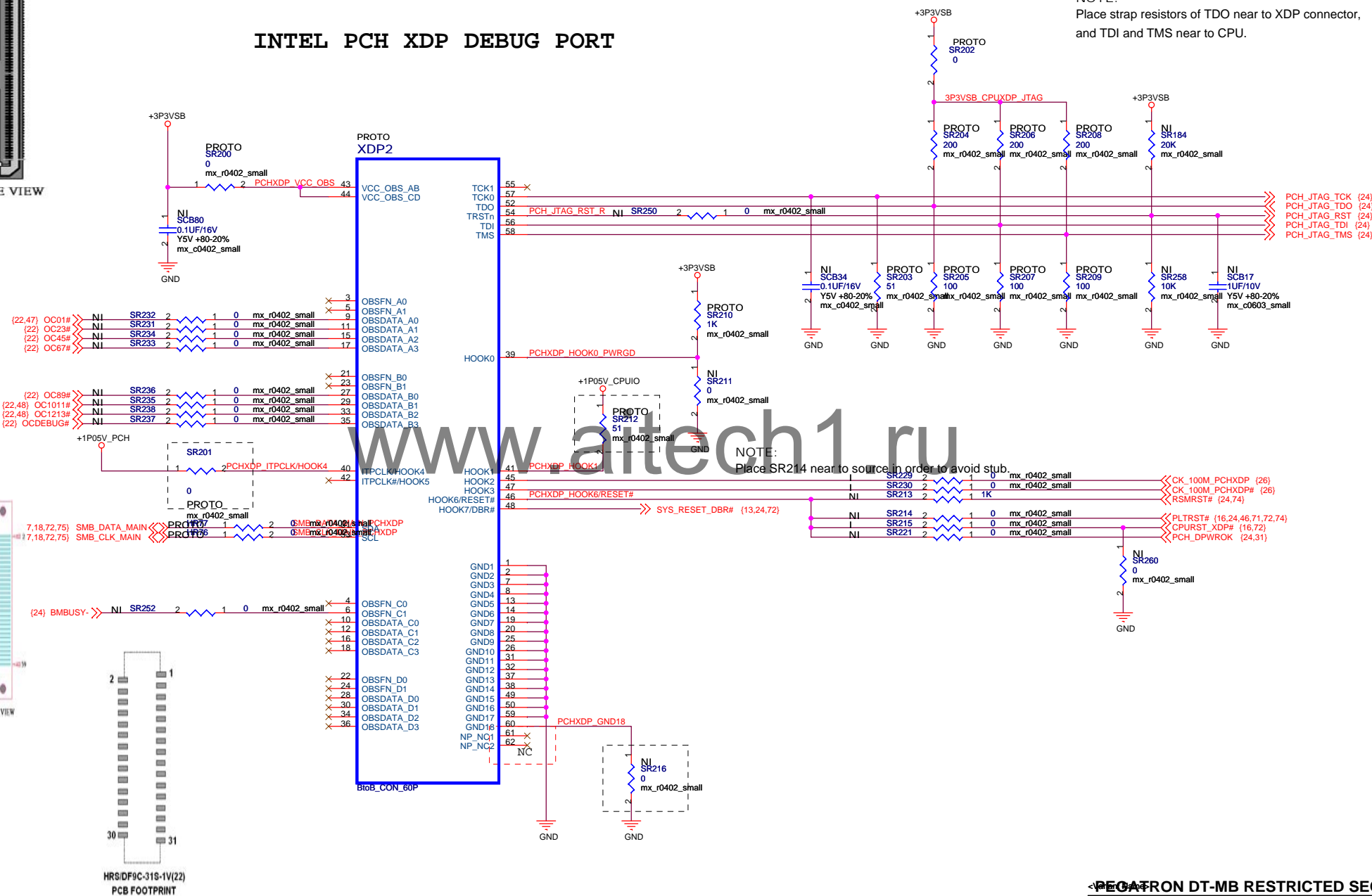
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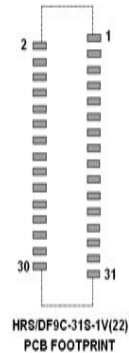
TOP SIDE VIEW

INTEL PCH XDP DEBUG PORT

NOTE:
Place strap resistors of TDO near to XDP connector,
and TDI and TMS near to CPU.



BOTTOM SIDE VIEW



PCB FOOTPRINT

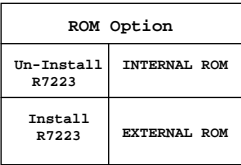
PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : PCH XDP DEBUG

Pegatron Corp. Engineer: Scott Chen

Size Project Name IPISB-SB

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